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- Application of fast-recovery epitaxial diodes in SMPS
- Survey of teletext transmission systems and Mullard decoders
- The TDA1071 IC in a.m./f.m. radio receivers
- System design aids for the 2650 microprocessor

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This issue of Mullard Technical Communications marks the 25th anniversary of its first publication in May 1952. The cover design symbolises the immense changes that have taken place in electronics during these 25 years, from the thermionic valves used in the hi-fi audio amplifiers of the 50's to the LSI microprocessor of present-day computer systems.

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Application of fast-recovery epitaxial diodes in switched-mode power supplies

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This article shows the requirements for fast-recovery diodes in switched-mode power supplies. Fast-recovery epitaxial diodes are introduced, and two calculations are included to illustrate their use in a forward converter switched-mode power supply.

INTRODUCTION

The increasing interest in switched-mode power supplies (SMPS) has led to the development of a whole new range of specially-designed components. High-voltage switching transistors, control integrated circuits, ferrite transformer cores, low-voltage and high-voltage electrolytic capacitors, and mains and output rectifier diodes, all intended specifically for use in switched-mode power supplies, are now available (Refs.1 to 5). Of these, the rectifier diodes used in the output circuit of the supply are particularly important. Firstly, they must be fast, since switched-mode power supplies normally operate at frequencies between 25 and 50kHz; secondly, they must have a low forward voltage, because in low-voltage switched-mode circuits this is the main factor limiting efficiency.

Recently, epitaxial technology has been used to produce rectifier diodes with forward voltages of less than 1V at full rated current, and recovery times of only 35 to 50ns. These are the BYW29, BYW30, BYW31, and BYW92 fast-recovery epitaxial diodes (FREDs), intended for use in switched-mode power supplies providing output voltages from 8 to 30V.

This article describes forward and push-pull converter circuits for switched-mode power supplies, and shows the advantages of fast-recovery epitaxial diodes in these kinds of application. Selection of particular devices for industrial circuits is considered in a later section.

FORWARD CONVERTER SWITCHED-MODE POWER SUPPLIES

Circuit operation

The basic circuit of a forward converter is shown in Fig.1. Voltage V_i is the d.c. supply voltage, which is switched at a high frequency (20 to 50kHz) by transistor TR_1. The primary winding of the transformer is in the transistor collector circuit. The current I_s from the secondary winding flows through diode D_2 and choke L_1 to supply the load; only the choke ripple current flows through the capacitor C_2. The voltage V_o across C_2 is the required smoothed output voltage. The output voltage can be regulated by feeding a proportion of V_o back to the control circuit of the power supply (not shown) which accordingly adjusts the mark/space ratio (duty cycle δ) of the transistor. The winding in series with D_1 returns the energy stored in the core to the supply when V_s is negative and there is no load, thus limiting the maximum collector voltage of TR_1 to twice V_i. This winding is bifilar wound with the primary to ensure low leakage inductance.

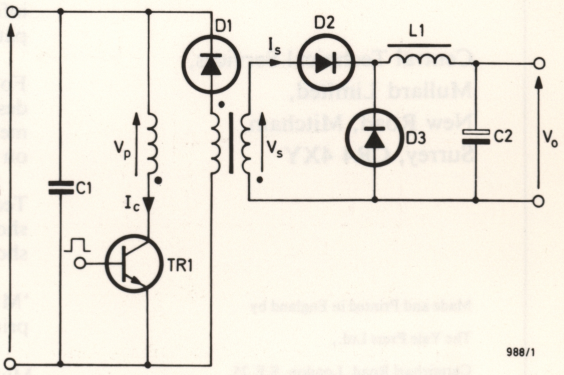

Fig.1 — Basic forward converter circuit

When TR_1 is turned on, current I_c flows in the transformer primary (Fig.2), and current I_s flows in the secondary through diode D_2, choke L_1, and the load. When TR_1 is turned off, D_2 turns off, and the current in L_1 now flows through the flywheel diode D_3.

Whenever current flows through either of the diodes, a voltage is dropped across that diode, as outlined below.

Forward voltage of diodes

The secondary voltage and diode current waveforms are shown in Fig.2. As the choke current always flows either through D_2 or D_3, the output voltage V_o is lower than would be expected by an amount equal to the forward voltage of either diode (assuming D_2 and D_3 to be the same). Thus:

$$V_o + V_F = V_s\delta, \qquad \ldots(1)$$

where V_F is the forward voltage of D_2 or D_3, and δ is the duty cycle. The power loss resulting from V_F is:

$$P_{loss} = V_F I_o, \qquad \ldots(2)$$

where I_o is the output current of the circuit. It is obvious that to minimise power loss and maximise efficiency, the forward voltages of diodes D_2 and D_3 must be as low as possible. In this respect, epitaxial diodes are superior to conventional double-diffused types because they have lower slope, or series, resistances and hence lower forward voltages, allowing the design of more efficient power supplies with smaller rectifier heatsinks.

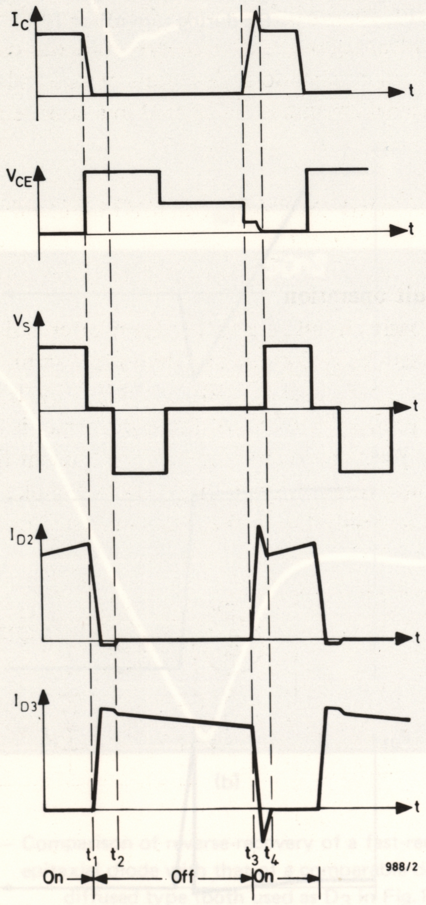

Fig.2 — Transistor current and voltage waveforms, and secondary voltage and current waveforms, of forward converter

Reverse recovery

The stored charge in the output rectifier diodes has a detrimental effect on the operation of a power supply during switching, as described below.

Switch-off

When TR_1 is on, D_2 is conducting and D_3 is off. When TR_1 is switched off, I_c falls and V_{CE} rises towards twice V_i, current in D_2 begins to fall, the voltage across L_1 reverses and increases until D_2 becomes reverse-biased. Current builds up in D_3 as the current in D_2 decreases, thus maintaining the current in L_1 almost constant. Thus from time t_1 to t_2, both D_2 and D_3 are forward-biased, and the secondary winding of the transformer is effectively short-circuited. This holds V_s at 0V until D_2 becomes reverse-biased. During the turn-off time, which is predominantly the reverse-recovery time of D_2, the secondary voltage V_s is zero, and therefore the magnetic flux in the transformer remains constant. It is essential that the reverse-recovery time of D_2 is small compared with the turn-off time of TR_1 to ensure that there is sufficient time for the demagnetising winding to reduce the flux to zero before TR_1 is again switched on. This reverse-recovery time can limit the upper operating frequency or maximum duty cycle of the power supply unless fast reverse-recovery diodes are used.

Switch-on

The reverse-recovery behaviour of D_3 is quite different from that of D_2 because it occurs during the turn-on of TR_1. At the instant TR_1 is turned on, there is no current flowing through the primary or secondary of the transformer. The current flowing in L_1 flows through D_3 (see Fig.2). When TR_1 is turned on, current begins to flow in

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The author wishes to thank M.C. Basell (formerly of Mullard Central Application Laboratory) who contributed the major part of the information in this article.

D_2 and that in D_3 decreases, maintaining the current in L_1 almost constant. With both D_2 and D_3 again forward-biased, the voltage on the secondary is zero. The rate of rise of current through the transformer leakage inductance, which can be considered as being in series with the primary, determines the voltage across the transformer input (V_p) and hence the collector-emitter voltage V_{CE} of TR_1. The current through the leakage inductance is the same as the collector current of TR_1. Therefore V_{CE} is determined by the rate of rise of collector current dI_c/dt. That is:

$$V_i = V_p + V_{CE},$$

and:

$$V_{CE} = V_i - L_L \frac{dI_c}{dt},$$

where L_L is the leakage inductance.

The rate of rise of I_c depends on the base drive to the transistor. With normal base drive, where the base current is approximately 0.1 to 0.2 of I_c, the rate of rise of I_c (20 to 50A/µs) is insufficient for the leakage inductance voltage to reach the level of the transformer input voltage, or:

$$V_i \neq L_L \frac{dI_c}{dt}.$$

Therefore TR_1 does not saturate during reverse recovery of D_3 (see Fig.3).

Fig.3 demonstrates the effect that the reverse-recovery time and stored charge have upon the transistor collector voltage. It shows in greater detail the transistor switch-on time, t_3 to t_4 in Fig.2. The peak reverse-recovery current of D_3 occurs between time t_3 to t_4 (the reverse-recovery time) on the I_{D3} waveform of Fig.2. This current flows through the secondary winding and diode D_2, and causes the peak on the waveform of I_{D2}. This peak has an effect upon the voltage and current in TR_1, as shown by Fig.3. When TR_1 is switched on, V_{CE} falls rapidly until D_2 becomes forward-biased (due to the increase in I_c and thus I_s), short-circuiting the secondary winding and causing V_{CE} to level out for the reverse-recovery time of D_3. This plateau occurs simultaneously with I_c max, causing a relatively large collector dissipation.

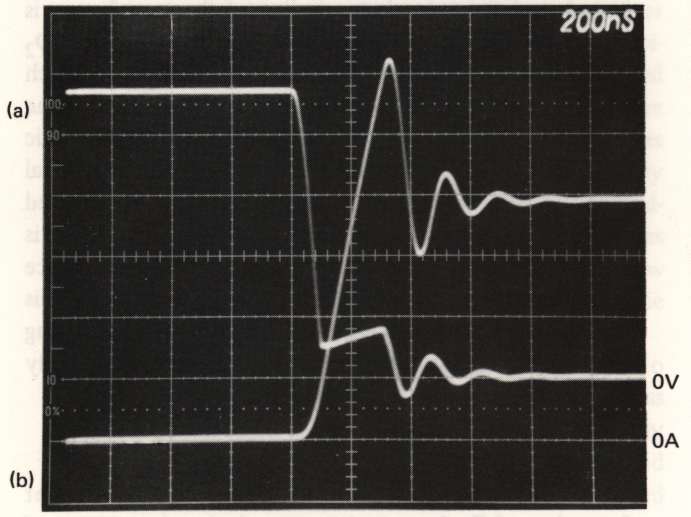

Fig.3 – Collector-emitter voltage and collector current of TR_1 during turn on:
(a) V_{CE} 10V/division
(b) I_c 1A/division
Horizontal scale 200ns/division

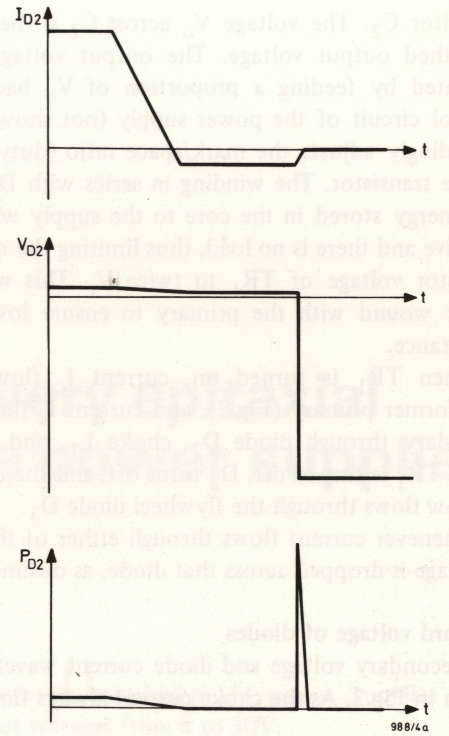

Fig.4a – Voltage, current, and power in diode D_2 during turn-off of TR_1

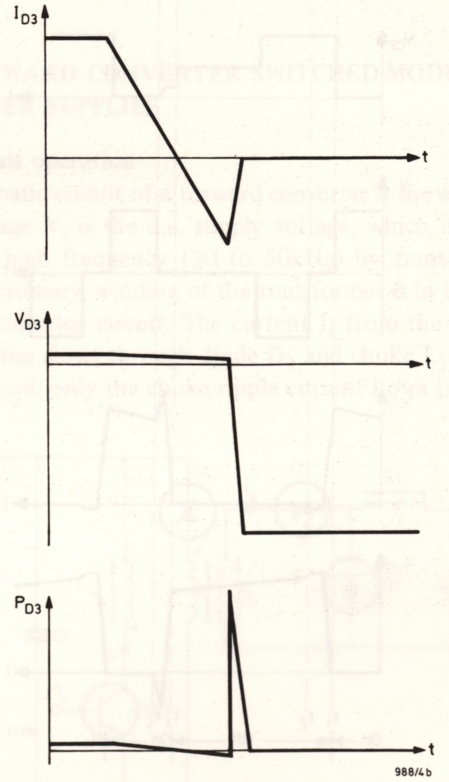

Fig.4b – Voltage, current, and power in diode D_3 during turn-on of TR_1

This dissipation during turn-on can be the main source of power loss in the transistor, caused not by any shortcomings in the transistor itself but by imperfections in the output diode characteristics.

A further disadvantage of the reverse-recovery in D_3 is that the spike produced in the primary circuit may result in malfunction of the current limit circuits operating on collector current. Appropriate measures must therefore be taken in the current limit circuit to nullify the effects of this spike. This further complicates the operation of the current limit circuit, creating problems which are difficult to overcome.

The reverse-recovery current I_R results in very little power loss in the diodes at switching because the power loss only occurs as I_R falls to zero, but as the fall-time of I_R is very short, the average power loss per cycle is negligible. This is shown in Figs.4a and 4b, which show the output diode current and voltage changes at switch-on and switch-off (see also Fig.2).

A comparison of the reverse recovery of an epitaxial diode with that of a double-diffused fast rectifier (both used as D_3 in Fig.1) is shown in Fig.5, showing the smaller stored charge and shorter reverse-recovery time of the epitaxial device.

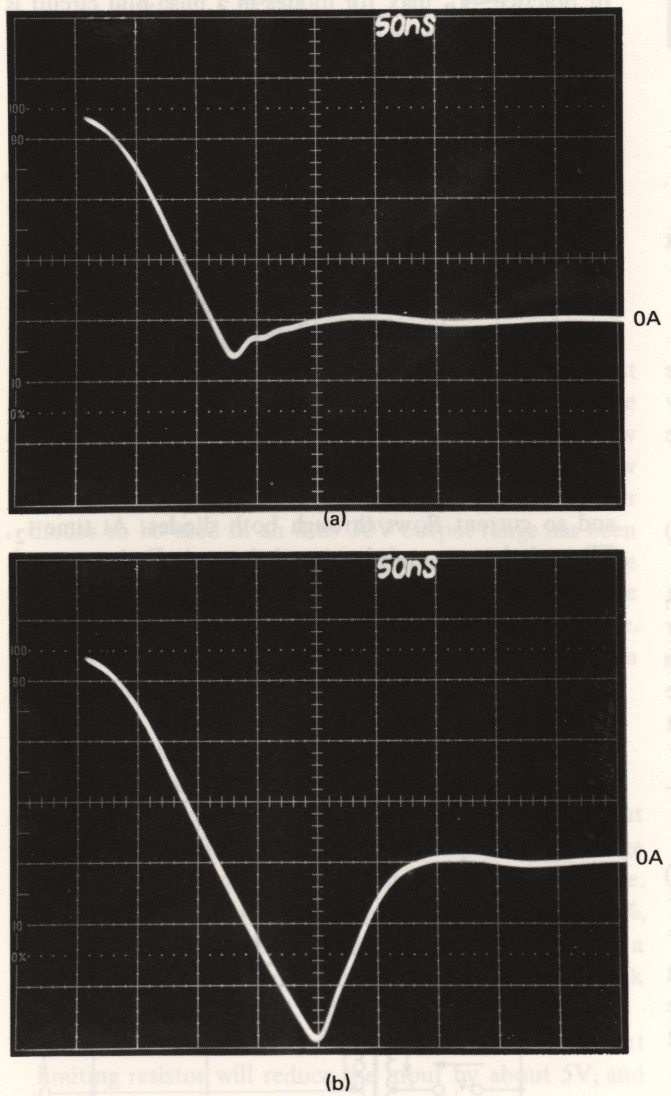

Fig.5 – Comparison of reverse-recovery of a fast-recovery epitaxial diode with that of a comparable double-diffused type (both used as D_3 in Fig.1):
(a) BYW31 epitaxial diode
(b) Double-diffused diode
Vertical scale 1A/division
Horizontal scale 50ns/division

Reduction of reverse-recovery current

The reverse-recovery current spike in the flywheel diode D_3 (and hence in the primary current) in a forward converter can be suppressed by placing an inductor in series with the flywheel diode (L_1 in Fig.6). The inductor limits the rate of fall of current to such an extent that the stored charge in the diode is removed before the current reverses, thus limiting I_R to a low value.

During the fall-time of the secondary current in the transformer, magnetising current is still flowing, returning energy to the input via the demagnetising winding. This reduces the power output capability of the power supply. However, by using a non-linear saturable inductor for L_1, the fall-time is very much reduced and the rate of fall is limited only as the diode current approaches zero. In this way, I_R is reduced almost to zero and the energy returned to the supply is minimised. A fast-recovery diode is, however, still essential to keep the size of the inductor small and to reduce the amount of energy

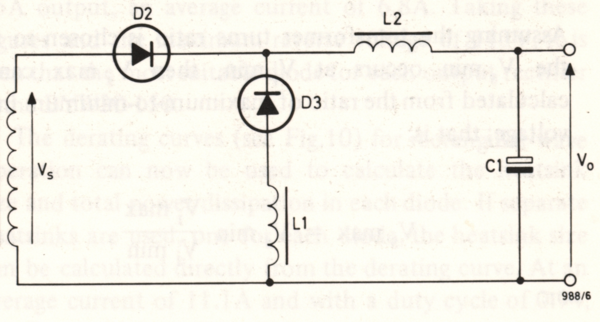

Fig.6 – Use of non-linear saturable inductor L_1 to suppress reverse-recovery current spike

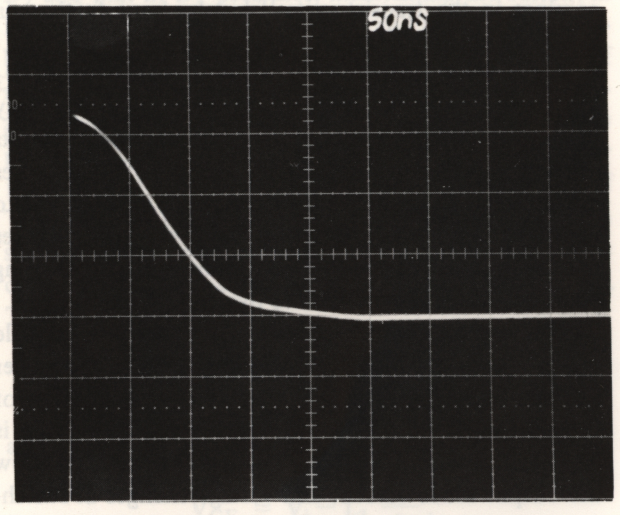

Fig.7 – Waveform of current in D_3, during turn-off, showing removal of spike
Vertical scale 1A/division
Horizontal scale 50ns/division

returned to the supply. The current waveform of D_3 at turn-off is shown in Fig.7.

Reverse voltage

The reverse voltage V_R of the non-conducting diode (either D_2 or D_3) in Fig.1 depends on the secondary voltage V_s and the forward voltage V_F across the conducting diode; that is:

$$V_R = V_s - V_F. \qquad \ldots (3)$$

The secondary voltage V_s is determined by the input voltage to the switching stage V_i and the transformer turns ratio. The maximum reverse voltage V_R max can therefore be calculated from the maximum input voltage and the transformer turns ratio. If the turns ratio is not known, V_R max can be calculated from Eq.1.

The minimum secondary voltage necessary to maintain the output voltage V_o is:

$$V_s \min = \frac{V_o + V_F}{\delta_{max}}. \qquad \ldots (4)$$

Assuming the transformer turns ratio is chosen so that the V_s min occurs at V_i min, then V_s max can be calculated from the ratio of maximum-to-minimum input voltage; that is:

$$V_s \max = V_s \min \frac{V_i \max}{V_i \min}, \qquad \ldots (5)$$

or:

$$V_s \max = \frac{V_o + V_F}{\delta_{max}} \cdot \frac{V_i \max}{V_i \min}, \qquad \ldots (6)$$

and:

$$V_R \max = \frac{V_o + V_F}{\delta_{max}} \cdot \frac{V_i \max}{V_i \min} - V_F. \ldots (7)$$

In a push-pull converter the duty cycle can theoretically vary between 0 and 1, and V_R max for each of the output rectifier diodes (for a centre-tapped transformer) is:

$$V_R \max = \frac{2(V_o + V_F)}{\delta_{max}} \cdot \frac{V_i \max}{V_i \min} - V_F. \qquad \ldots (8)$$

In practice, V_R max for diodes in a push-pull circuit is the same as for those in an equivalent forward converter.

PUSH-PULL SWITCHED-MODE POWER SUPPLIES

Push-pull power supplies operate in a similar manner to the forward converter, except that both diodes at the output turn off in the same way as D_3 in the forward converter. The switching stage of a push-pull supply is shown in Fig.8, and the secondary voltage and current waveforms are shown in Fig.9.

When TR_1 is on, D_1 conducts and D_2 is reverse-biased. When TR_1 switches off at t_1, I_{D1} begins to fall and I_{D2} begins to rise. Both are forward-biased between t_1 and t_2, so the secondary winding is effectively short-circuited and V_s is 0V. The voltage across L_1 reverses and so current flows through both diodes. At time t_2, TR_2 switches on, and the stored charge in D_1 is removed, causing the spike in I_{D2}. Diode D_2 now conducts and D_1 is reverse-biased. At t_3, TR_2 switches off and both diodes become forward-biased, as before. At t_4, TR_1 switches on and the stored charge in D_2 is removed, causing the spike in I_{D1}.

The current at which D_1 and D_2 turn off is only half the output current, therefore the stored charge is less than in a forward converter with the same output current.

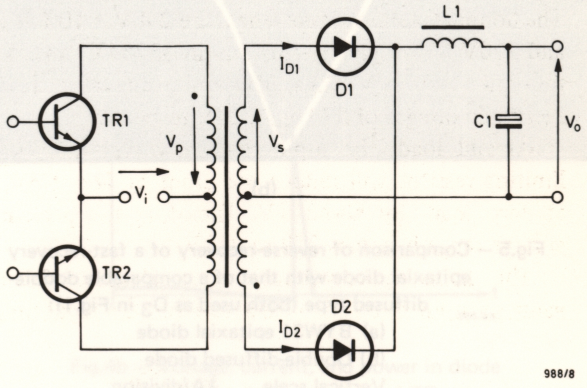

Fig.8 – Basic push-pull converter circuit

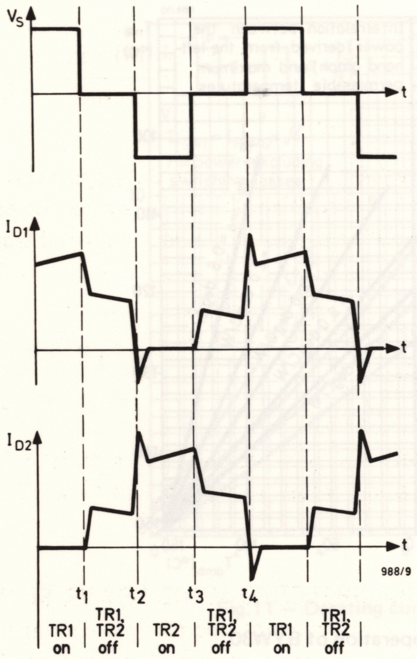

Fig.9 – Secondary voltage and diode current waveforms of push-pull converter

FAST-RECOVERY EPITAXIAL DIODES

The above discussion of rectifier diodes in the output circuits of switched-mode power supplies shows that the requirements are for an appropriate combination of low forward voltage with short reverse-recovery time, a low stored charge, and low cost. The optimum solution for diodes to be used in an 8 to 30V output range has been found to be fast-recovery epitaxial diodes (Ref.6). The Table at the end of this article gives abridged data for the range of fast-recovery epitaxial diodes currently available. Two calculations, which illustrate the correct diode for a particular application, follow.

Diode selection for 28V output forward converter operating from 220 to 240V mains

The forward converter considered here is a mains-input circuit giving 28V, 15A output. The input voltage range can be calculated from the variation in mains voltage. The nominal mains voltage ranges are 240V + 10% – 20%, and 220V ±15%, giving a maximum of 264V r.m.s. and a minimum of 187V r.m.s. These are equivalent to peak rectified voltages of 373 and 264V respectively.

At full load, the input rectifier bridge and current limiting resistor will reduce the input by about 5V, and at zero load, by about 1V. Therefore the peak input voltage range becomes 259 to 372V.

The mains ripple voltage can be calculated from the value of input smoothing capacitor and the load; that is:

$$V_2 = \left[V_1{}^2 - \frac{2Pt}{C} \right]^{1/2}, \qquad \ldots (9)$$

where V_1 is the peak mains voltage, V_2 is the peak mains voltage less the ripple voltage, P is the input power, t is the time for which the input bridge is not conducting, and C is the input smoothing capacitance (Ref.7). For 50Hz full-wave rectified mains, t will be about 8.5ms, or when one random half-cycle is missing, 18ms. Assuming that the power supply is 80% efficient and that the input capacitance is 2μF per watt of output power, the ripple voltage is:

$$V_2 = \left[259^2 - \frac{2 \times 1.25 \times 18 \times 10^{-3}}{2 \times 10^{-6}} \right]^{1/2}.$$

$$= 211\text{V}.$$

Thus, allowing for ripple, the power supply input range becomes 211 to 372V.

The maximum practical duty cycle at minimum input voltage can be taken as 0.45 and, taking the forward voltage drop in the diodes to be about 1V, the maximum reverse voltage is, from Eq.7:

$$V_R \max = \left(\frac{28 + 1}{0.45} \right) \frac{372}{211} - 1.0,$$

$$= 113\text{V}.$$

The minimum duty cycle under steady-state conditions can be calculated from the maximum duty cycle δ_{max} and the input voltage range. Thus:

$$\delta_{min} = \delta_{max} \frac{V_i \min}{V_i \max}, \qquad \ldots (10)$$

$$= 0.45 \times \frac{211}{372} \qquad = 0.26.$$

The maximum average steady-state current in each output rectifier can now be calculated. At maximum input voltage, the flywheel diode D_3 has a duty cycle of 0.74. For an output current of 15A, therefore, the average current will be 11.1A. At minimum input voltage, diode D_2 has a duty cycle of 0.45, giving, at 15A output, an average current of 6.8A. Taking these figures and the maximum reverse voltage of 113V, it is seen that the most suitable diode for each output rectifier is the BYW30-150.

The derating curves (see Fig.10) for rectangular-wave operation can now be used to calculate the heatsink size and total power dissipation in each diode. If separate heatsinks are used, one for each diode, the heatsink size can be calculated directly from the derating curve. At an average current of 11.1A and with a duty cycle of 0.74, the flywheel diode D_3 will have a power dissipation of 11W, and, assuming an ambient temperature of 60°C, will require a heatsink with a thermal resistance of

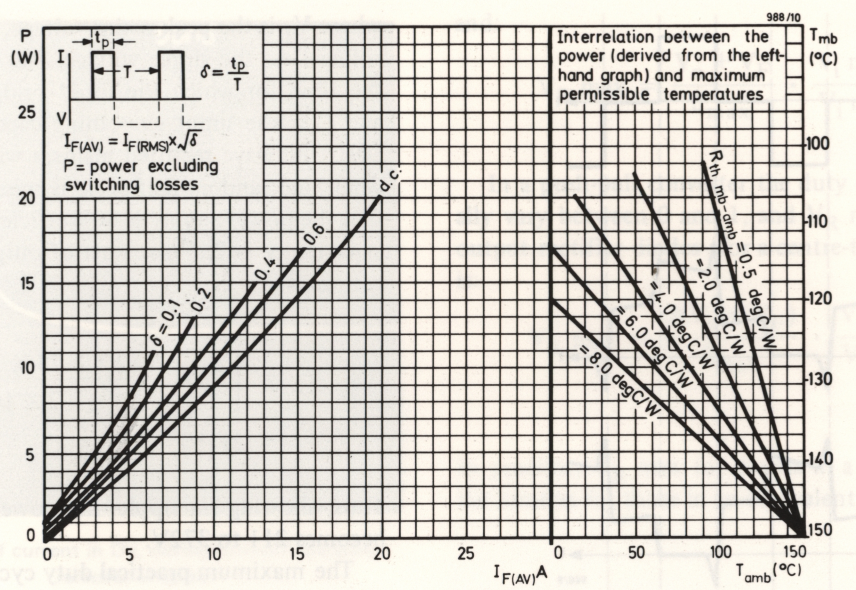

Fig.10 — Derating curves for rectangular-wave operation of BYW30

6degC/W. Similarly, diode D_2 at an average current of 6.8A and with a duty cycle of 0.45 will require a heatsink with a thermal resistance of 10degC/W.

If both diodes are mounted on the same heatsink, the total power dissipation can be calculated from the derating curve using the d.c. curve and an average current of 15A, since only one diode is conducting at any time. This gives a value for the total power dissipation of 14.2W. Assuming again an ambient temperature of 60°C, the derating curve indicates that a heatsink with a thermal resistance of about 4degC/W is required. This is a larger value than is actually necessary since it assumes that all power is dissipated in only one of the diodes. A more accurate value can be found by calculating the temperature rise for each diode junction, knowing the thermal resistance of each diode under the worst-case conditions; that is, a duty cycle of 0.74 for D_3 and 0.26 for D_2. However, in practice the approximate value found using the simpler method is sufficiently accurate.

It should be noted that if the power supply described here is required to operate in a constant-current mode at full output current, then the maximum duty cycle of the flywheel diode D_3 will be almost 1.0 and the maximum average current will be 15A. A BYW31-150 will then be necessary for this diode.

Diode selection for 12V output forward converter operating from 50V Post Office supply

The circuit considered here is a forward converter running from a –50V supply to give 12V 8A output. The input voltage range is assumed to vary between –40 and –60V. The maximum practical duty cycle can again be taken to be 0.45, and with a maximum forward voltage drop in the diodes of 1V, the maximum reverse voltage can be calculated from Eq.7, that is:

$$V_R \max = \left(\frac{12+1}{0.45}\right)\frac{60}{40} - 1.0,$$

$$= 42V.$$

The minimum duty cycle under steady-state conditions is, from Eq.10:

$$\delta_{min} = 0.45 \times \frac{40}{60},$$

$$= 0.30.$$

The maximum average steady-state current in each rectifier can now be calculated. At maximum input voltage, the flywheel diode D_3 has a duty cycle of 0.70. For an output current of 8A, therefore, the average current will be 5.6A. At minimum input voltage, D_2 has a duty cycle of 0.45 giving, at 8A output, an average current of 3.6A. The most suitable diode for each output rectifier is thus the BYW29-50.

The derating curves (see Fig.11) for rectangular-wave operation can now be used to calculate the heatsink size and total power dissipation in each diode. When one heatsink is used for each diode, with an average current of 5.6A and a duty cycle of 0.70, D_3 will have a power dissipation of 6W. Assuming an ambient temperature of 60°C, it will require a heatsink with thermal resistance of 14degC/W. Similarly, D_2 at an average current of 3.6A and a duty cycle of 0.45 will require a heatsink of 16degC/W.

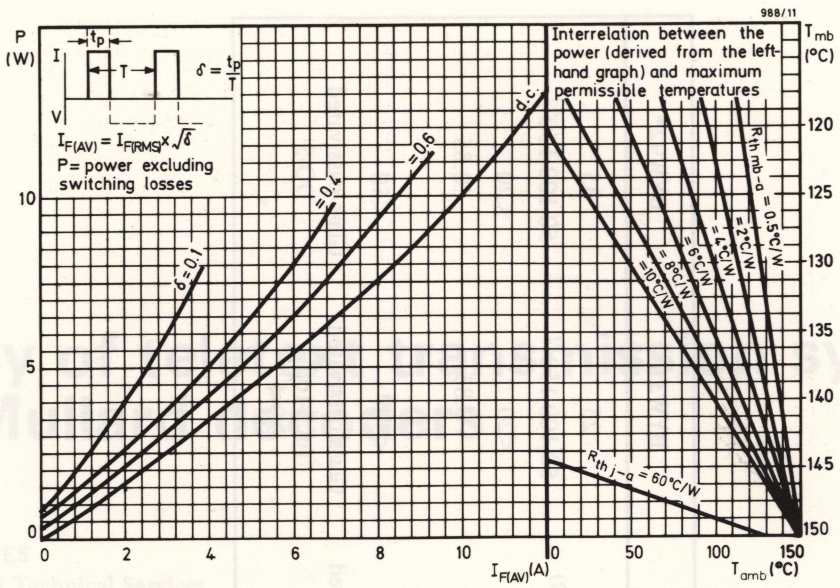

Fig.11 — Derating curves for rectangular-wave operation of BYW29

If both diodes are mounted on the same heatsink, the average current is 8A. The total power dissipation will thus be 7.5W and the heatsink will need a thermal resistance of 8degC/W.

It should again be noted that if the power supply is required to operate in a constant-current mode at full output current, the maximum duty cycle of D_3 will be almost 1.0 and the maximum average current will be 8A. A BYW30-50 will then be necessary for this diode.

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The Table of abridged data for the current range of fast-recovery epitaxial diodes is given overleaf.

Abridged Data for Fast-recovery Epitaxial Diodes

			BYW29	BYW30	BYW31	BYW92*
Average forward current	$I_{F(AV)}$	(A)	7	12	25	35
Repetitive peak inverse voltage	V_{RRM}	(V)	50,100,150$^{1)}$	50,100,150$^{2)}$	50,100,150$^{3)}$	50,100,150$^{4)}$
Recovered charge	Q_s	(nC)	<15	<15	<20	<20
Average forward voltage	V_F at $I_{F(AV)}$ ($T_j = 125°$)	(V)	0.85	0.85	0.85	0.85
Recovery time	t_{rr}	(ns)	<35	<35	<50	<50
Encapsulation			Glass-passivated eutectic-bonded DO-220	Glass-passivated DO-4	Glass-passivated 'rock-top' DO-4	Glass-passivated DO-5

*Under development at time of publication (April 1977)

1) BYW29-50, BYW29-100, BYW29-150
2) BYW30-50, BYW30-100, BYW30-150
3) BYW31-50, BYW31-100, BYW31-150
4) BYW92-50, BYW92-100, BYW92-150

Survey of teletext transmission systems and Mullard decoders

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A brief history of teletext transmission systems is given, including descriptions of CEEFAX, ORACLE, and Viewdata. The prototype decoders developed by Mullard are described. Reference is also made to future trends and the Mullard LSI decoder system, incorporating full remote control, which is planned for release shortly.

INTRODUCTION

The domestic television systems operated by the BBC and IBA each now carry additional communication 'channels', completely independent of the normal transmission service. The information for these channels is transmitted in the form of digitally-encoded alphanumeric data, and is carried on some of the television lines in the field flyback period that do not contain picture information. Specially-developed circuits can then extract this data, store it, and reconstitute it as a display. In this way, pages of text and graphical information based on an alphanumeric format can be transmitted and received. The IBA began test transmissions of such alphanumeric information in April 1973, and the BBC in June 1973. The IBA system of transmission was named ORACLE (Optional Reception of Announcements by Coded Line Electronics), and the BBC system was named CEEFAX (see facts).

Initially, the only similarity between the two systems lay in the data transmission sequence which consisted of a synchronising pattern, a unique address, and ASCII-coded data. (ASCII is the American Standard Code for Information Interchange.) Mullard developed prototype adaptor units for decoding the early CEEFAX and ORACLE transmissions and for use with standard domestic television receivers. Mullard also coined the word 'teletext' (text at a distance) as a generic term for all transmission-reception-display systems of the CEEFAX/ORACLE type.

It soon became highly desirable for the two teletext systems to be standardised, and accordingly a Working Group was set up by BREMA (British Radio Equipment Manufacturer's Association) to examine the differences between CEEFAX and ORACLE and to recommend a standard transmission system. As a result, in July 1974 a new unified system was agreed, different from either of the original versions, and incorporating a number of refinements to improve flexibility. The names CEEFAX and ORACLE have been retained for the information services from the BBC and IBA respectively, although the transmission coding systems are identical. It is this unified system that is described here.

By December 1974, Mullard had designed a new laboratory-prototype decoder system for the acquisition and display of CEEFAX and ORACLE transmissions. The overall design of this system has been described in a series of publications (see Refs.1 to 8). The prototype system consisted of eight digital boards and one linear board, and is described in outline later in this article.

Mullard are currently developing complex large-scale integrated (LSI) circuits in N-MOS technology for specific use in decoding teletext transmissions. This latest design is for a versatile decoder, which can occupy a single compact printed-wiring board, for use with domestic receivers, and coupled with a comprehensive remote control system.

Although the Mullard decoder systems are intended initially for use with a television receiver for the acquisition, storage, and display of broadcast teletext information, both systems can be adapted to be fed from other data sources. An example of such a teletext source is 'Viewdata', the experimental system now operated by the British Post Office. In this, the data is transmitted along normal telephone lines from a central computer, the service having some characteristics that are quite different from the television systems, as described later.

During the period of several years over which these data transmission-reception systems have been developed for use as practicable domestic and professional services, Mullard has been in close liaison with the BBC, IBA, BREMA, and the Post Office. This close contact has helped to ensure arrival at a system which is convenient both for transmission and reception; the reception, which includes decoding the data, is of course largely the concern of setmakers and their component suppliers.

THE UNIFIED CEEFAX AND ORACLE TRANSMISSION SYSTEM

Detailed information on the unified CEEFAX and ORACLE system may be found in Ref.9. The main features are, however, summarised here, so that the operation of the Mullard prototype decoder system may more easily be explained.

Television data lines for teletext transmission

It was mentioned earlier that the data for the teletext transmissions is carried by some of the unused lines of the television picture during the flyback period. The allocated lines are called 'data lines'. At present, for CEEFAX and ORACLE, two data lines above the normal displayed picture are used in every field, and these are lines 17 and 18 in the even field, and lines 330 and 331 in the odd field. (The standard television raster is briefly described later under 'Displayed page'.) The data can be seen on a maladjusted receiver, having inadequate picture height, as rows of bright-up dashes at the top of the picture. The data rate of 6.9375Mbits/s is 444 × the line frequency. This rate is such that data for a complete row of forty teletext characters may be inserted on each data line: with two data lines per field, this means that a full page of twenty-four rows can be transmitted in twelve fields, or less than one quarter of a second.

It is possible that, in the future, up to sixteen lines could be used for the transmission of data instead of the present two. The data could be allocated to lines 6 to 22 in the even field, and lines 319 to 335 in the odd field. The Mullard LSI decoder system will be capable of processing data from up to sixteen lines should these become available. An increase in the number of data lines would result in a faster net data rate, which would create two options for data transmission: either an increase in the number of pages with the same access time, or a substantial reduction in the time required to transmit the present amount of information. Although sixteen lines are potentially available for data transmission, it would require international agreement for their use; some of these lines are at present used for other purposes, such as the remote control of relay transmitters.

Transmission sequence

The information on each data line consists of two basic parts. The first part is an address code which tells the decoder unit at the receiver on which row (one of twenty-four) the information is to be displayed. The second, major, part is the character data, a sequence of character codes representing the particular symbols to be displayed. It is also necessary to identify the information as belonging to a particular page. This could be done by having a page code on each data line, but this would occupy valuable space on the data line. A neater method of identifying pages has therefore been adopted: this necessitates defining two types of data line, a 'normal' data line and a 'page header'.

The page header is designated as the top row (row 0) of the display, and carries information according to a standard format. It contains the page number and address, together with other information such as the date, the time, and the title 'CEEFAX' or 'ORACLE'. This information allows the decoder to recognise the page selected by the viewer, and prepare the memory in the decoder for receiving information. Subsequent 'normal' data lines contain information for the same page as indicated by the page header, and therefore on 'normal' data lines the only address information necessary is the row number. The end of transmission of a particular page is indicated by the arrival of another page header for a new page.

Normally pages are transmitted in sequence, and real clock time is transmitted with the page header and can be displayed at the top of the displayed page. Page headers may be repeated by the transmitting authorities at the clock time 'seconds' changeover to make the transmitted 'time' information more accurate. This potentially allows the time changeover to be transmitted in the nearest available field blanking period, giving a time accurate to ±10ms. The pages themselves can be transmitted in any order, and so if a rapidly changing subtitle is required then that subtitle page may be transmitted more frequently than other pages.

Format of the data lines

The position of the teletext data on the data lines is shown in Fig.1. Simple NRZ (non-return-to-zero) coding of the digital data is used, binary '0' being represented by black level (0%) and binary '1' as 66% of peak white level (see Ref.9).

The format of the data on a data line is shown in Figs.2a (normal) and 2b (page header). The transmission

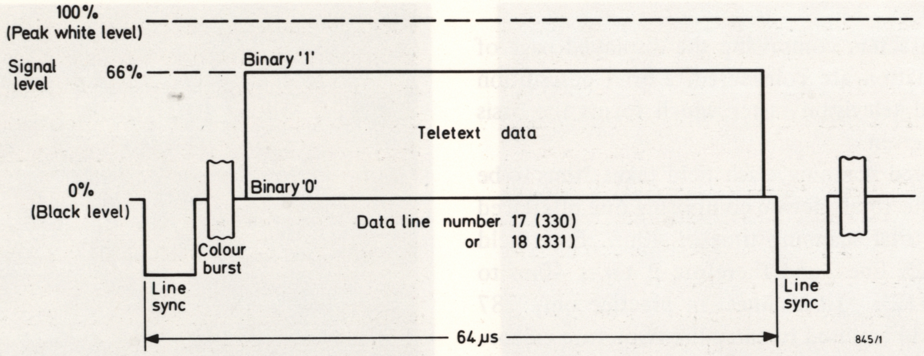


Fig.1 – Position of teletext data on television lines in the field flyback period

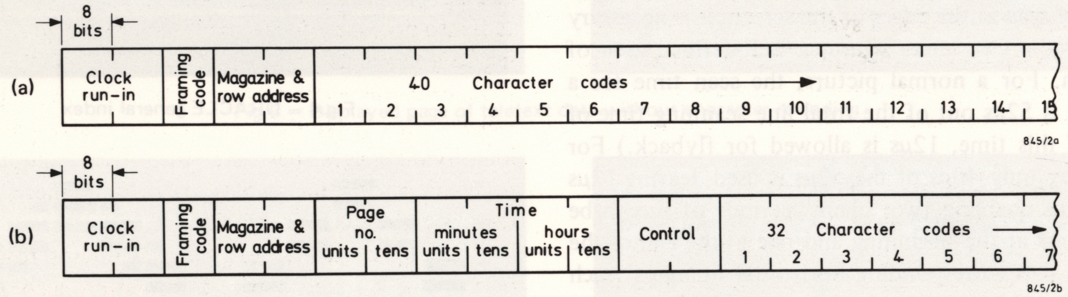


Fig.2 – Format of broadcast teletext data:
(a) on a normal line; (b) on a page header

is organised as groups of 8 bits of data, and the significance of each bit is determined by its position in the data stream. It is necessary to provide a clock signal to clock the data into a digital decoder circuit, and this must be synchronised with the incoming data. The first two groups of information on a data line therefore consist of a clock run-in sequence (101010 etc. with the maximum number of transitions), which allows the data clock in the decoder to be started and synchronised. The next 8-bit group of data is a framing code or 'start' code. This unique sequence accurately defines the point at which counting of the incoming data bits must begin. After this point, information can be clocked into the decoder, the clock pulses being counted to determine the function of each bit.

The first two groups of 'proper' data contain the row address and the magazine address. These are protected by Hamming codes (Ref.1). The use of Hamming codes allows a single bit error in each 8-bit group to be detected and corrected. If there are two errors in an 8-bit group, the information in the data line is rejected. Thus the row address is adequately protected, so that under normal signal conditions information is unlikely to be written into the wrong row.

In a 'normal' data line, as shown in Fig.2a, the next forty groups of 8 bits consist of the teletext character codes for the forty characters of a row. Each character has 7 bits plus one parity bit. The first eight 'character' positions on a page header, however, contain the page and time address as shown in Fig.2b. Page and time addresses are transmitted in BCD form, this being compatible with the decimal-based user selection controls. All of these addresses are also protected with Hamming codes.

The remaining information on the page header is displayed as the top row on the screen. This information consists of the page number and the real clock time, duplicated as character codes, together with the day, date, and 'CEEFAX' or 'ORACLE', transmitted as shown in Fig.3.

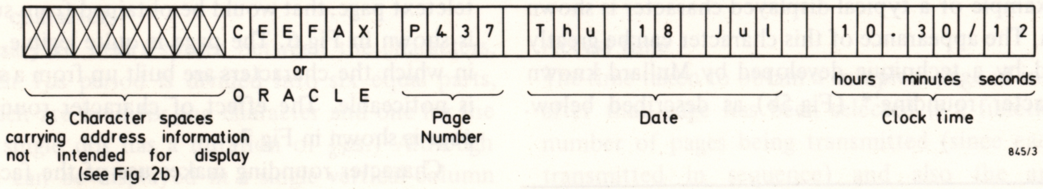


Fig.3 – Page header display

Displayed page

Before the characters comprising the displayed page of teletext information are considered, a brief description of the standard television raster which forms the basis for this page is given.

With interlaced scanning, each field takes 20ms to be scanned, and the total picture comprising one interlaced frame takes a total scanning time of 40ms. Each field consists of 312½ lines, and therefore it takes 40ms to display (2 X 312½ =) 625 lines. In practice only 287 lines of each field are used to carry the tv picture video.

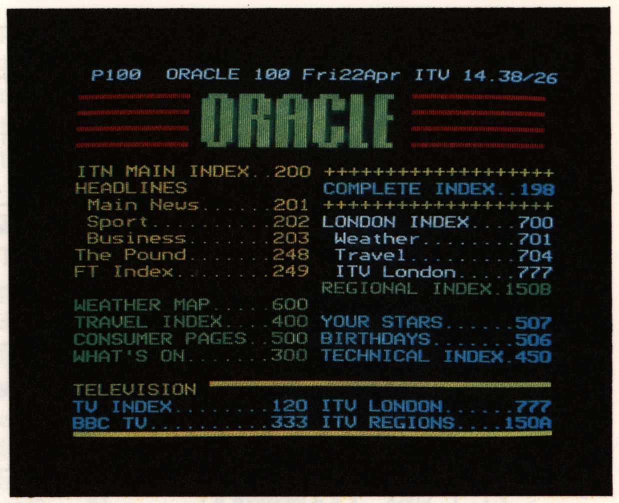
Because the display obtainable from a typical domestic receiver is unlikely to be ideal, particularly in terms of linearity of scan at the edges of the screen, it is necessary to display the characters within a well-defined area of the screen. For a normal picture, the scan time for a single line is 52μs out of the total line scanning time of 64μs. (Of this time, 12μs is allowed for flyback.) For data display only 40μs of the 52μs is used, leaving 12μs 'spare', thus enabling two 'blank' periods of 6μs to be inserted, one at the beginning and one at the end of the line scan. The corresponding horizontal 'margins' each occupy about 11½% of the total line scan. These margins permit partial overscanning of the tube, and a consequent improvement in the quality of the displayed characters. Similar margins are inserted in the vertical display, and in every field only 240 lines out of the 312½ lines are used for data display. The display starts at line 48 and ends at line 288, and the margins at the top and the bottom of the screen each occupy about 10% of the total vertical display.

Displayed characters

A full page of information (displayed on the screen one page at a time) consists of twenty-four rows of characters with forty characters to each row. In the 40μs (display) period, therefore, each character has a duration of 1μs. Ten out of the 240 lines in each field (twenty lines in the interlaced frame) are used for the display of one row of characters.

Ninety-five different alphanumeric characters are transmitted; these are upper-case and lower-case letters, numbers, and various punctuation marks and other symbols. An example of a page of teletext information displayed on the screen of a television receiver is shown in Fig.4. The characters are transmitted as 7-bit teletext character codes, giving 2^7 or 128 possibilities for each character.

An example of a typical displayed character is shown in Fig.5a. The appearance of this character can be greatly improved by a technique developed by Mullard known as 'character rounding'* (Fig.5b) as described below.



P100 ORACLE 100 Fri22Apr ITV 14.38/26

ORACLE

ITN MAIN INDEX..200 ++++++++++++++++++++++
HEADLINES COMPLETE INDEX..198
Main News......201 ++++++++++++++++++++++
Sport..........202 LONDON INDEX....700
Business.......203 Weather.........701
The Pound.......248 Travel..........704
FT Index........249 ITV London.....777
REGIONAL INDEX.150B

WEATHER MAP.....600
TRAVEL INDEX....400 YOUR STARS......507
CONSUMER PAGES..500 BIRTHDAYS.......506
WHAT'S ON.......300 TECHNICAL INDEX.450

TELEVISION
TV INDEX........120 ITV LONDON......777
BBC TV..........333 ITV REGIONS....150A

Fig.4 – ORACLE general index

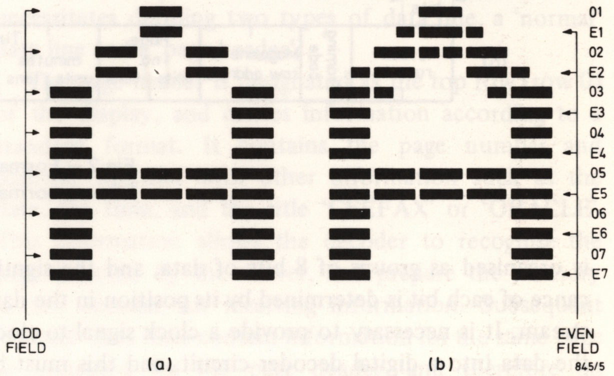


Fig.5 – Typical displayed character:
(a) without character rounding,
(b) with character rounding

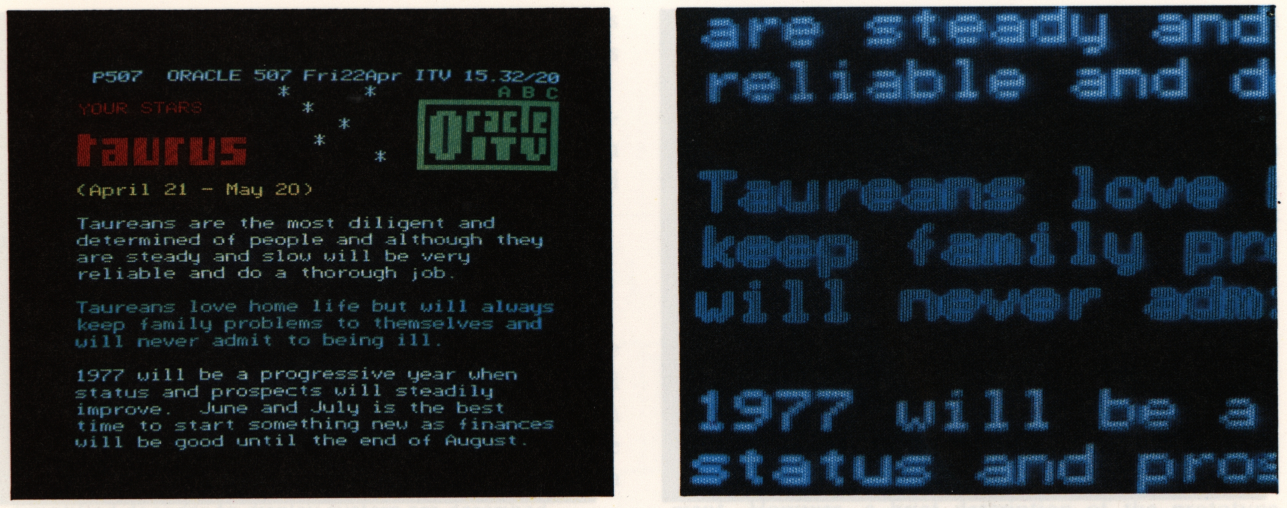
Apart from the ninety-five displayed symbols, some 'control characters' can also be transmitted; these are not themselves displayed but control other facilities of the system.

Character rounding

The teletext decoder converts the character codes into a serial output of dot information to modulate the brightness of the picture tube during the scan. A ROM (read-only memory) in the decoder contains character information on a 7 X 5 dot matrix basis. This information is converted by a character generator into a video signal which is then supplied to the tube.

An example of the type of display, in the form of a teletext page, that would be obtained from such a system is shown in Fig.6. The page is quite legible, but the way in which the characters are built up from a series of dots is noticeable. The effect of character rounding on this page is shown in Fig.7.

Character rounding makes use of the fact that all the letters, numbers, and symbols in normal use are made up from a series of lines. The character rounding circuit modifies the video signal from the character generator when a diagonal line is being generated so that a smoother display is obtained. No increase in the bandwidth of the video amplifier in the receiver is required for this improvement. In effect, the dot resolution of each character is doubled in both the horizontal and vertical directions. A teletext character generated on the 7 X 5 dot matrix appears with a 14 X 10 dot resolution.



P507 ORACLE 507 Fri22Apr ITV 15.32/20
A B C
YOUR STARS
taurus
Oracle ITV
(April 21 - May 20)

Taureans are the most diligent and
determined of people and although they
are steady and slow will be very
reliable and do a thorough job.

Taureans love home life but will always
keep family problems to themselves and
will never admit to being ill.

1977 will be a progressive year when
status and prospects will steadily
improve. June and July is the best
time to start something new as finances
will be good until the end of August.

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Taureans love
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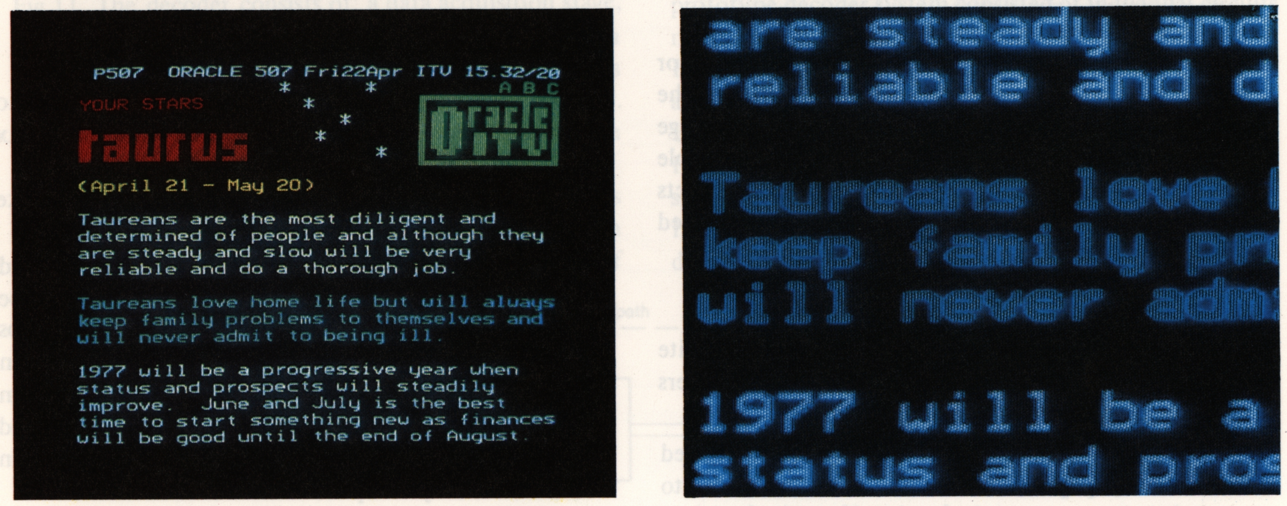
1977 will be a
status and pros

Fig.6 – Displayed page of teletext data without character rounding



P507 ORACLE 507 Fri22Apr ITV 15.32/20
A B C
YOUR STARS
taurus
Oracle ITV
(April 21 - May 20)

Taureans are the most diligent and
determined of people and although they
are steady and slow will be very
reliable and do a thorough job.

Taureans love home life but will always
keep family problems to themselves and
will never admit to being ill.

1977 will be a progressive year when
status and prospects will steadily
improve. June and July is the best
time to start something new as finances
will be good until the end of August.

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Taureans love
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will never adm
1977 will be a
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Fig.7 – Displayed page of teletext data with character rounding

Full details of the display of these characters, together with the principles of character rounding are given in Ref.10.

Spacing of characters

It is necessary to insert spaces between the characters, and so each 1μs period is divided into six equal parts, five of which are used for the character and one for the space. (A single dot has a duration of $\frac{1}{6}\mu$s.) Although seven dots can be displayed in a single vertical column within the matrix, letters like lower-case g and j descend below the base line and it is therefore necessary to provide a further two dots for the formation of the 'tails' of these letters. Out of the ten lines used for each row, a single television line space remains between the bottoms of these letters and the tops of the characters in the line below.

Number of pages

Each television channel is capable of providing up to 800 individual teletext pages, arranged in eight groups or 'magazines'. The pages are selected from the numerical sequence 100 to 899. An example of a CEEFAX general index page is shown in Fig.8.

Access time

The time taken to obtain a complete page of information after that page has been selected is a function of the number of pages being transmitted (since each page is transmitted in sequence) and also the amount of information in each page: subtitles, with only one row

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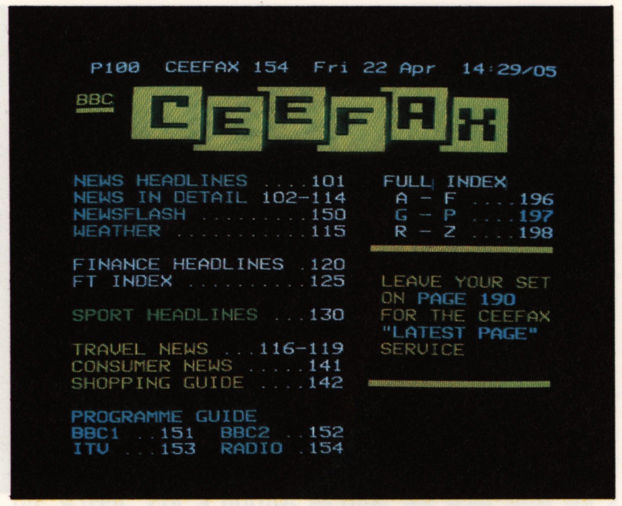
*U.K. Patent No.1343298, and Patent Application No.22687/74



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P100  CEEFAX 154  Fri 22 Apr  14:29/05
BBC  CEEFAX

NEWS HEADLINES ....101     FULL INDEX
NEWS IN DETAIL 102-114      A - F ....196
NEWSFLASH .........150      G - P ....197
WEATHER ...........115      R - Z ....198

FINANCE HEADLINES .120
FT INDEX ..........125     LEAVE YOUR SET
                           ON PAGE 190
SPORT HEADLINES ...130     FOR THE CEEFAX
                           "LATEST PAGE"
TRAVEL NEWS ...116-119     SERVICE
CONSUMER NEWS .....141
SHOPPING GUIDE ....142

PROGRAMME GUIDE
BBC1 ..151  BBC2 ..152
ITV ...153  RADIO .154
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Fig.8 – CEEFAX general index

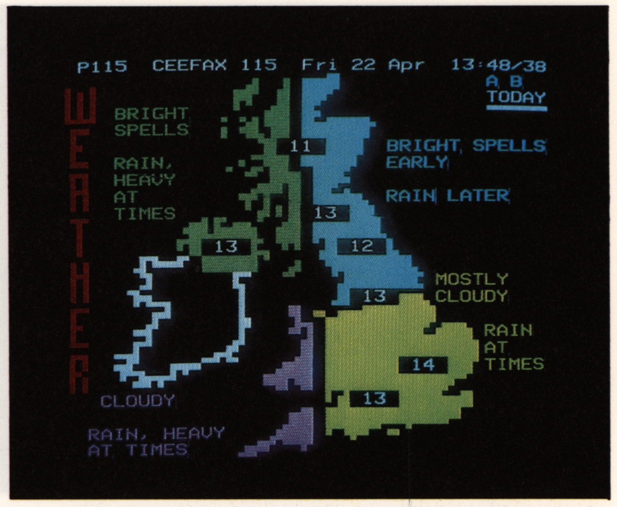


Fig.10 – Specimen CEEFAX weather map

of information, consume less transmitting time. For example, if 100 full pages are being transmitted, then the maximum access time is about 25s with an average waiting time of 12.5s. These figures are only applicable when two data lines are in operation. The possible effects of an increased number of data lines were mentioned earlier; that is, more pages or shorter access time.

Additional facilities

In addition to the transmission of pages of simple white alphanumeric data, the broadcast teletext system offers a number of refinements.

1) Timed pages: Clock-time information is transmitted with every page, and the viewer can also select to receive a page at a particular time if required.
2) Subtitles and newsflashes: Control characters can be transmitted which allow the normal television video signal to be blanked out in certain positions and a 'box' to be formed round a teletext-generated caption as shown in Fig.9.
3) Colours: Control characters can be transmitted to display individual words in any of the available six colours (and white).
4) Flash: Control characters can be transmitted to make individual words flash repetitively.
5) Graphics: In addition to the normal symbols provided by the character generator, control characters can be transmitted to allow the construction of simple maps and diagrams from a series of dots on the screen. An example of the display of graphics is shown in Fig.10. Graphics and alphanumerics may be mixed on the same page, and graphics can be coloured in the same way as alphanumerics.
6) Concealed display: This control character can be transmitted to give the option of suppressing part of the display until the next colour control character is transmitted, or until the end of a row. For example, the answer to a question can be concealed by the viewer until it is required.
7) Suppression of header: This control character can be transmitted to suppress the header on selected pages.
8) 'Update' header: This control character can be transmitted to indicate when a page has been updated.
9) Out-of-sequence header indicator: This character can be transmitted whenever it is necessary to transmit pages out of sequence, such as subtitles or repeated index pages. The indicator makes it possible to avoid discontinuities in the display of rolling page numbers.
10) Inhibit: This character can be transmitted on all occasions when the teletext format is being used to convey signals other than teletext, and it can thus be used to inhibit the display of meaningless pages.
11) Automatic double-height characters: This control character causes selected characters to be displayed at twice their normal height.

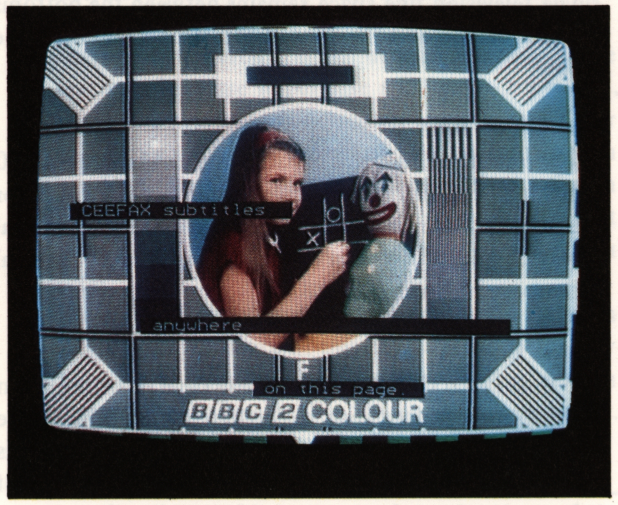


Fig.9 – Teletext subtitle displayed with picture

12) Graphics hold: Different coloured areas in graphics can be joined up without gaps between the graphics characters.
13) Background colour control character: The transmission of this character allows a background of an appropriate colour to be displayed behind selected coloured characters.

DECODER-TO-DISPLAY SYSTEM

It was mentioned in the Introduction that the prototype decoder system and the new LSI decoder system could both be adapted to be fed from data sources other than teletext. Before some of these additional sources are considered, the functions of the principal sections of a simplified decoder-to-display system are described.

The principal sections of such a system are shown in Fig.11. The decoder consists of: a data acquisition stage, a memory, and a character generator. The display unit (a television receiver, monitor, or other display system) is driven by the video output from the character generator. In broad terms, the functions of the system shown in Fig.11 can be termed *grab, store,* and *display.*

Although, as indicated in Fig.11, the video drive is derived from a teletext transmission (video output from r.f. and i.f. stages), the memory would be capable of handling data, through suitable acquisition stages, from a variety of other sources.

In the Mullard prototype decoder system, the output from the data acquisition stage, in the form of character codes, is fed into a RAM (random access memory). The parallel character information from the RAM is fed into ROM devices in the character generator. The ROMs themselves contain character information on a 7 X 5 dot matrix basis, and this is used to produce the required alphanumeric display.

MULLARD PROTOTYPE TELETEXT DECODER SYSTEM

The Mullard prototype teletext decoder system will be superseded by the LSI system currently under development. However, a brief description of the prototype system is given here for the sake of completeness. The prototype decoder system consisted of individual circuits mounted on nine printed-wiring boards, as described in Refs.1 to 8. An experimental teletext decoder, designed and constructed in the Mullard Central Application Laboratory, and based on these circuits, is shown in Fig.12. As can be seen, the decoder was not, in this form, suitable for building in to a domestic television receiver. It had been designed with maximum flexibility for development purposes, and no attempt was made to

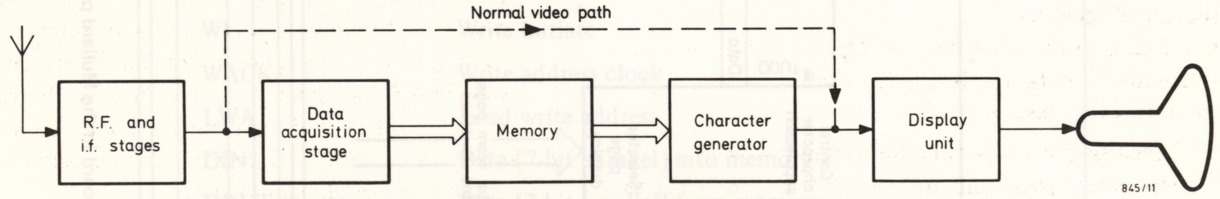


Fig.11 – Simplified decoder-to-display system

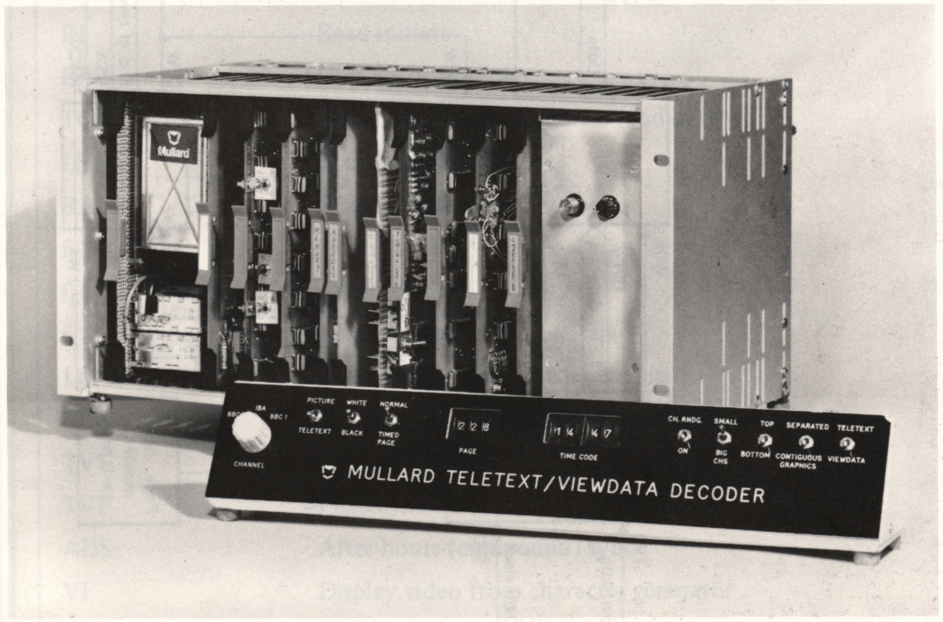


Fig.12 – Experimental decoder for teletext constructed on 19in rack

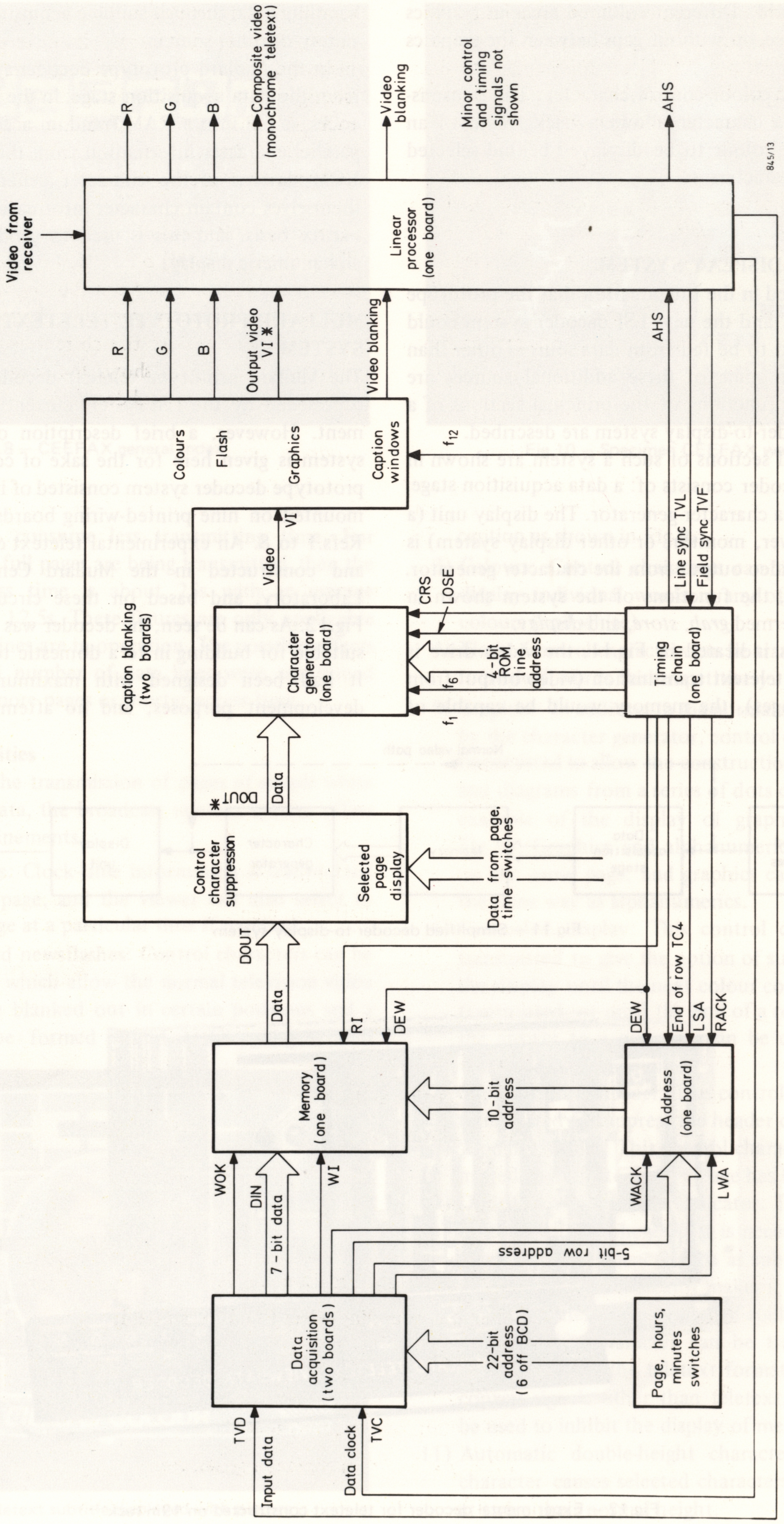

Video from receiver
R
G
B
Composite video (monochrome teletext)
Video blanking
Minor control and timing signals not shown
AHS
Linear processor (one board)
R
G
B
Output video VI*
Video blanking
AHS
Caption blanking (two boards)
Colours
Flash
Graphics
Caption windows
f12
Video
VI
Character generator (one board)
CRS
LOSE
f1
f6
4-bit ROM line address
Timing chain (one board)
Line sync TVL
Field sync TVF
DOUT*
Data
Control character suppression
Selected page display
Data from page, time switches
DOUT
Data
RI
DEW
DEW
End of row TC4
LSA
RACK
Memory (one board)
10-bit address
Address (one board)
WOK
DIN
WI
WACK
LWA
7-bit data
5-bit row address
Data acquisition (two boards)
22-bit address (6 off BCD)
Page, hours, minutes switches
TVD
Input data
Data clock
TVC
8LS/13

Fig.13 – Organisation of digital boards and linear board in the Mullard prototype teletext decoder system

reduce its size to achieve commercial acceptability.

The circuit boards in the prototype system can be broadly divided into eight digital types and one linear type, as shown in Fig.13. A brief description of the functions of each board is given below.

Digital boards

The interfacing between the digital boards and the linear board in the decoder system is shown in Fig.13. Most of the signals in the digital system are known by abbreviations: a list of these and their meanings is given in the Table. The operation of the digital system is described in Ref.1. The functions of the digital boards are described below.

Data acquisition boards

Two boards are used for the data acquisition circuit (Ref.6). The input signal to the digital part of the teletext decoder system consists of a serial data stream TVD together with an associated data clock TVC. The circuit processes the incoming information, and arranges for the data selected by the viewer to be written into the memory. The circuit provides various 'write control' and timing signals for the memory, and the row address of each data line is supplied to the address circuit. Error checking of the addresses (Hamming codes) and character data (parity) is incorporated.

Memory (RAM) board

The memory (RAM) board (Ref.3) stores the character codes as they come in from the data acquisition circuit during the data entry period, and supplies them to the character generator in the correct sequence during the display cycle. Fig.14 shows the memory (RAM) board used in the experimental decoder.

Address board

The address board (Ref.3) is used to convert from the 5-bit row address (one of twenty-four) to the correct storage location in the memory (10-bit address). The

List of Abbreviations of Signals

TVD	Input (serial) data
TVC	Input data clock
WOK	Write O.K.
WI	Write initiate
WACK	Write address clock
LWA	Load write address
DIN	Data (7-bit parallel) into memory
DOUT	Data (7-bit parallel) from memory
DOUT*	DOUT after modification by caption blanking board
RI	Read initiate
DEW	Data entry window
TC4	M.S.B. of ROM line address (end of row)
LSA	Load starting address
RACK	Read address clock
f_1	1MHz clock
f_6	6MHz clock
f_{12}	12MHz clock
LOSE	Load output shift register enable
CRS	Character rounding select (= odd/even field)
TVL	Line sync
TVF	Field sync
AHS	After-hours (compound) sync
VI	Display video from character generator
VI*	VI after modification by caption blanking board

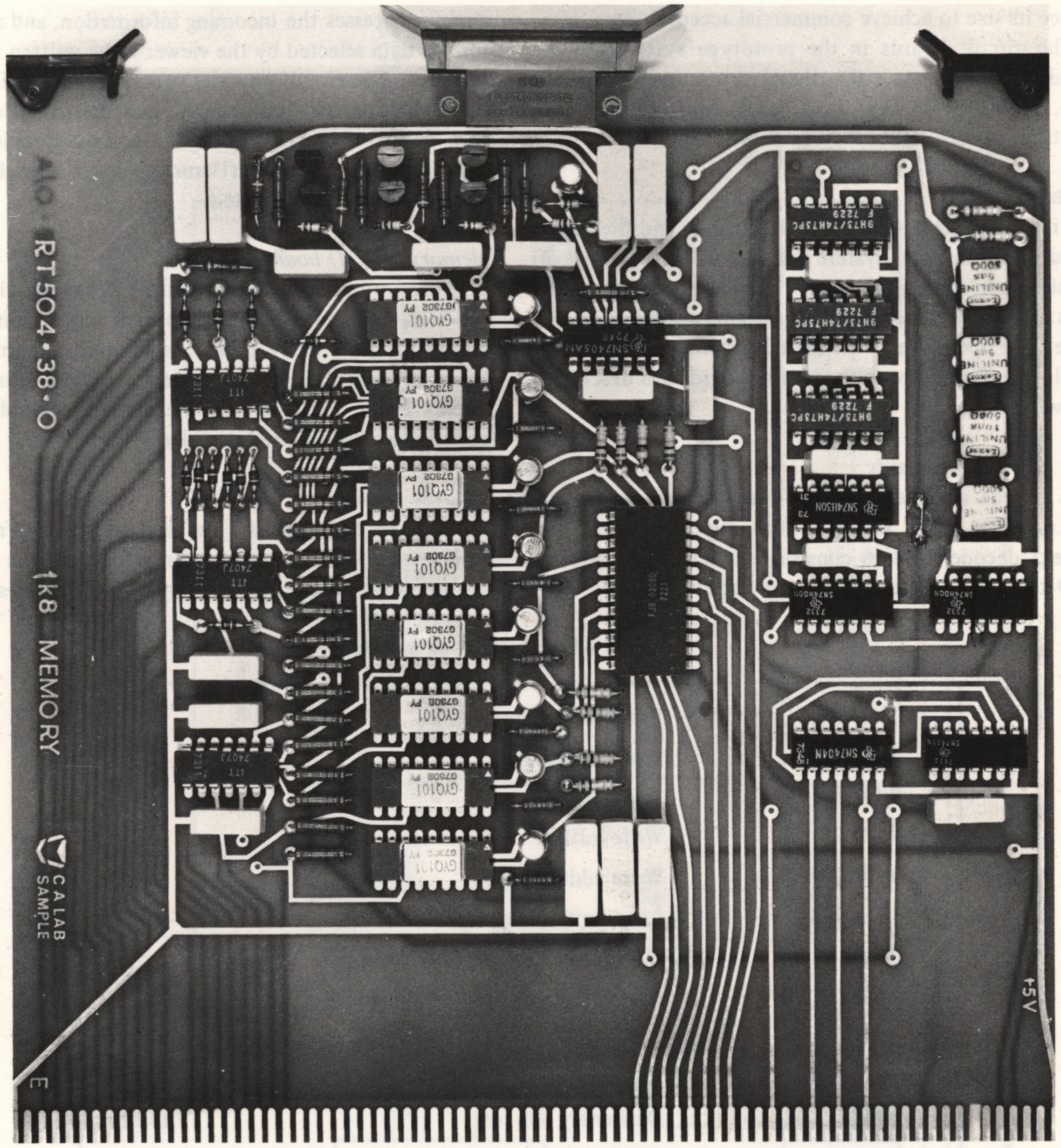


Fig.14 – Prototype memory (RAM) board

circuit multiplies the row address by 40 to find the location in the memory of the first character in that row: this presets the memory address counter. The address counter is then clocked on at character rate to obtain the storage locations of the next 39 characters.

Timing chain board

The timing chain board (Ref.4) provides control and timing signals for the television receiver or display unit, and also for the data acquisition circuit.

Caption blanking boards

Two boards are used for the caption blanking circuit (Ref.5). The boards include circuits for the various refinements of the CEEFAX and ORACLE broadcasts. The functions provided by the caption blanking circuit include: control character suppression, colours, 'flash', caption boxes, graphics, and selected page display. These functions are fully described in Ref.5.

Character generator (ROM) board

The character generator (ROM) board (Ref.2) converts the parallel teletext encoded character information from the RAM board to a serial output of dot information to modulate the television tube brightness during scan. The ROMs themselves contain character information on a 7 × 5 dot matrix basis; however, the ROM board contains additional (character rounding) circuitry which effectively increases the resolution to 14 × 10 dots (Ref.10).

Linear board

The single linear board (Ref.8) contains the linear processor circuit. This extracts the teletext data signals from the incoming video waveform and generates synchronising and timing waveforms for application to the digital boards. The circuit also processes the video character signals generated by the digital boards, thereby providing several switched options for display on the screen of the display unit. A monochrome output signal suitable for the modulation of a u.h.f. carrier is provided as an alternative to the red, green, and blue (RGB) character output signals. These output signals can be coupled, through a suitable video interface circuit, to the display unit used for the teletext display.

A switched-mode power supply for the complete decoder system is described in Ref.7.

The forthcoming LSI system has been based to some extent on the prototype decoder system. However, although some of the circuit functions of the two systems are in some ways comparable, the LSI system will provide several additional facilities including full remote control. The new system will also be more flexible than the prototype decoder.

ADDITIONAL SOURCES OF DATA

The foregoing description has been related largely to CEEFAX and ORACLE transmitted through the television channels. Alternative sources of data and modes of transmission can, however, be envisaged still using the television receiver as a means of display. The classification of such alternative data sources is considered next.

Data transmission systems can be broadly classified into three types:

1) interactive,
2) semi-interactive,
3) non-interactive.

Interactive systems: In interactive systems a two-way or multi-way exchange of information can take place. In a simple interactive system the interaction can take place between a user and a computer, an operation similar to that of a computer and its terminal. In more complex systems the user can receive data, modify its content, and retransmit these modifications, through a central computer, to update the data received by other users.

Semi-interactive systems: In these systems the user can demand on-store information from the source, but cannot modify its content. No feedback of information can therefore occur in these systems.

Non-interactive systems: CEEFAX and ORACLE are themselves, at present, available only as non-interactive systems and are therefore typical examples. A required page of information can be selected, but the user must wait until this information has been received from the total sequential transmission of pages. Any controlling options are limited to acceptance and rejection at the receiving end of the transmission system.

In practice, a particular system may be both interactive and semi-interactive, as is the 'Viewdata' system. It is this system that is described first as an additional source of data for the teletext decoder systems.

VIEWDATA

General description

The British Post Office began pilot trials of their Viewdata system in January 1976. The system provides on-line access to a database of information through an adapted television receiver and a telephone line. The principal parts of the overall Viewdata network are shown in Fig.15.

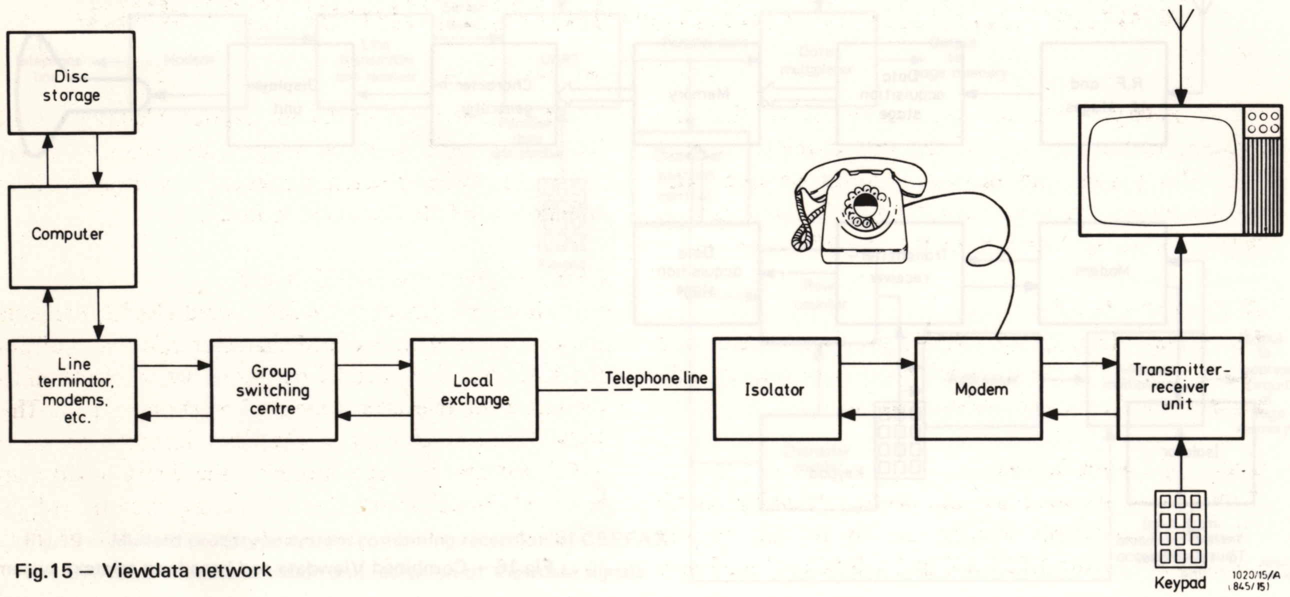


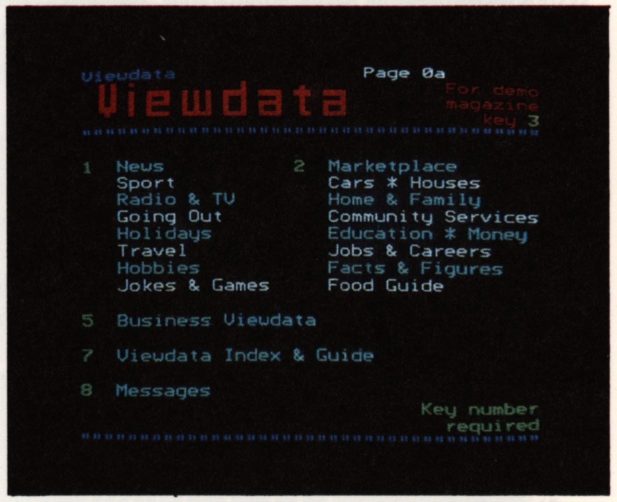
Fig.15 – Viewdata network

The receiving end of a standard system consists of an isolator, a modem, a subscriber telephone or an alternative automatic dialling unit, and a transmitter-receiver unit to which the television receiver and a keypad are connected. (The isolator ensures electrical isolation between the subscriber's equipment and the telephone line.) As shown in Fig.15, the Viewdata link can be established between the subscriber's equipment and a central computer through the conventional telephone network.

The displayed page format is identical to that of broadcast teletext; that is, forty characters in each row and twenty-four rows to a page. It is therefore possible to combine the Viewdata and broadcast teletext display facilities at the receiving end. Fig.16 shows a simplified block diagram of such a combined system, based on the teletext-only system shown in Fig.11.

During the present trials, the Post Office Datel 600 service (Ref.11) provides the data link, through the ordinary telephone line, between the user and the central computer. Two data rates are used at present: 1200bits/s for data transmitted from the computer and 75bits/s for data transmitted by the user. These data rates are considerably slower than the data rate for CEEFAX and ORACLE (6.9375Mbits/s) because of the electrical frequency limitations of the telephone line. However, despite having a faster data rate, the broadcast teletext data is at present carried by only two lines in every field. It is difficult to compare the time taken to select and display individual pages from each system because of the fundamental differences between the two methods of data transmission.

To link up with Viewdata, the user must first dial the local number of the system, either manually by using a subscriber telephone, or automatically by means of an 'auto-dial' key on the keypad. On receipt of the call, a high-pitched tone will be heard in the handset receiver of the telephone or from the loudspeaker in the television receiver. When the tone has been received, the 'data' button on the telephone must be pressed to transfer the incoming data to the transmitter-receiver unit. Where a telephone is not used, a key having a similar function to this button can be incorporated in the keypad. When the transmitter-receiver unit is brought into operation the Viewdata title page will be displayed on the television screen, and the user will then be requested to key-in a user number and a pass number. When this data is accepted, a 'greetings' page is displayed, containing: a greeting to the user, the date and time of the last connection to Viewdata, an indication of any 'message pages' awaiting the user's attention, and general messages from the Viewdata system itself. The user can then use the keypad to select the main index page or any other individual page. A typical Viewdata index page is shown in Fig.17.



```
Viewdata                      Page 0a
 Viewdata                    For demo
                             magazine
                                key 3

1  News               2  Marketplace
   Sport                 Cars * Houses
   Radio & TV            Home & Family
   Going Out             Community Services
   Holidays              Education * Money
   Travel                Jobs & Careers
   Hobbies               Facts & Figures
   Jokes & Games         Food Guide

5  Business Viewdata

7  Viewdata Index & Guide

8  Messages
                               Key number
                                 required
```

Fig.17 – Typical Viewdata index page

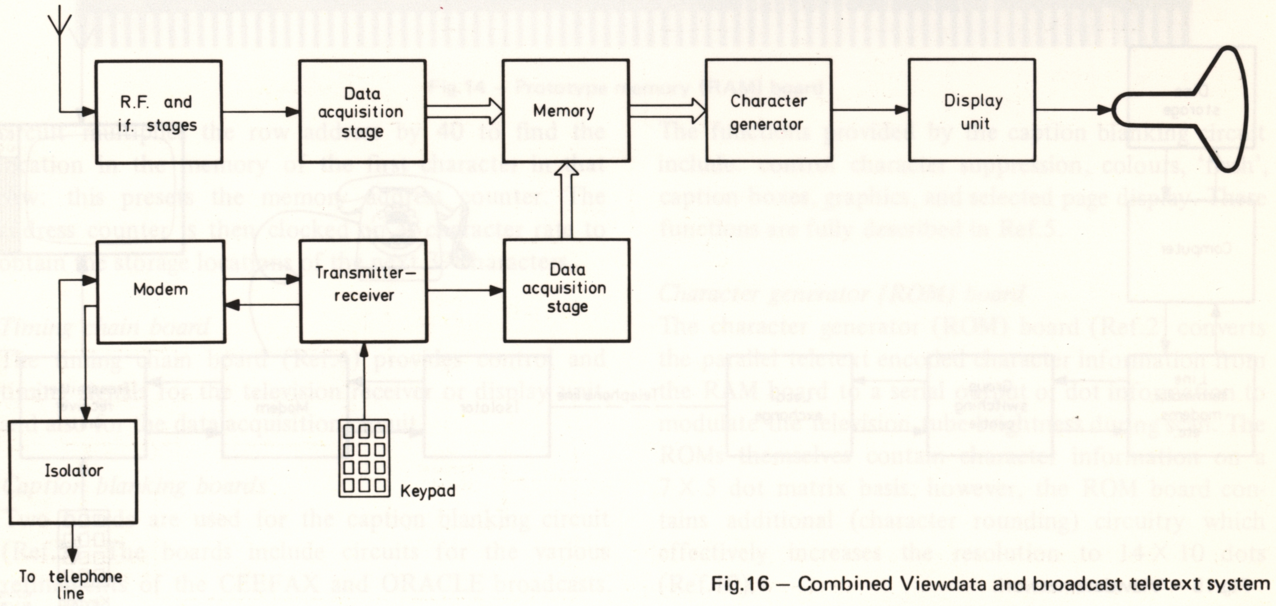


Fig.16 – Combined Viewdata and broadcast teletext system

Keypads and page selection

Two types of keypad can be used with the Viewdata system: a simple numeric type, or a full alphanumeric type. A typical layout of a simple numeric keypad is shown in Fig.18. When the Viewdata main index page is displayed, one of ten categories of information can be selected by one of the digits on the keypad. After this selection, a further index will be displayed, and so the selection can be continued until the desired page is located. The system has the technical capability of providing an unlimited number of pages of information. If the user knows the number of a particular page, then this page can be selected directly by keying the instruction *N#, where N is the page number. The remaining instructions are given below:

*# to recall a previous page,

*00 to recall the current page. This instruction would be used where data corruption has occurred during the transmission,

*0# to return to the main index,

** to delete miskeyed errors.

A variety of message services are available from the Viewdata system. A somewhat limited service is available for use with the numeric keypad, where numeric information can be inserted into pre-worded messages, such as;

'I shall be arriving on the . . . train'.

The transmitted message is held on store until the addressee next operates his or her system. Notification of any messages is given on the 'greetings' page, as mentioned earlier.

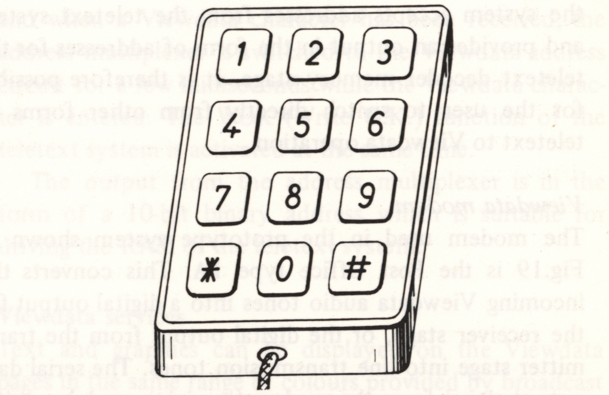


Fig.18 – Typical numeric keypad for selection of Viewdata pages

The alphanumeric keypad, containing a number of additional function keys, has several advantages over the simple numeric type, including the provision to send self-composed messages to other Viewdata users. The specialised user can also gain access to the calculation facilities of the central computer.

Future keypads could also contain an 'auto-dial' key. This function key would take the place of the telephone dial, as mentioned earlier. The circuit associated with this key could also enter the user number and pass number automatically.

Viewdata transmit-receive system

The principal stages of a Mullard prototype Viewdata transmit-receive system are shown in Fig.19. It can be seen that the address multiplexer at the output end of

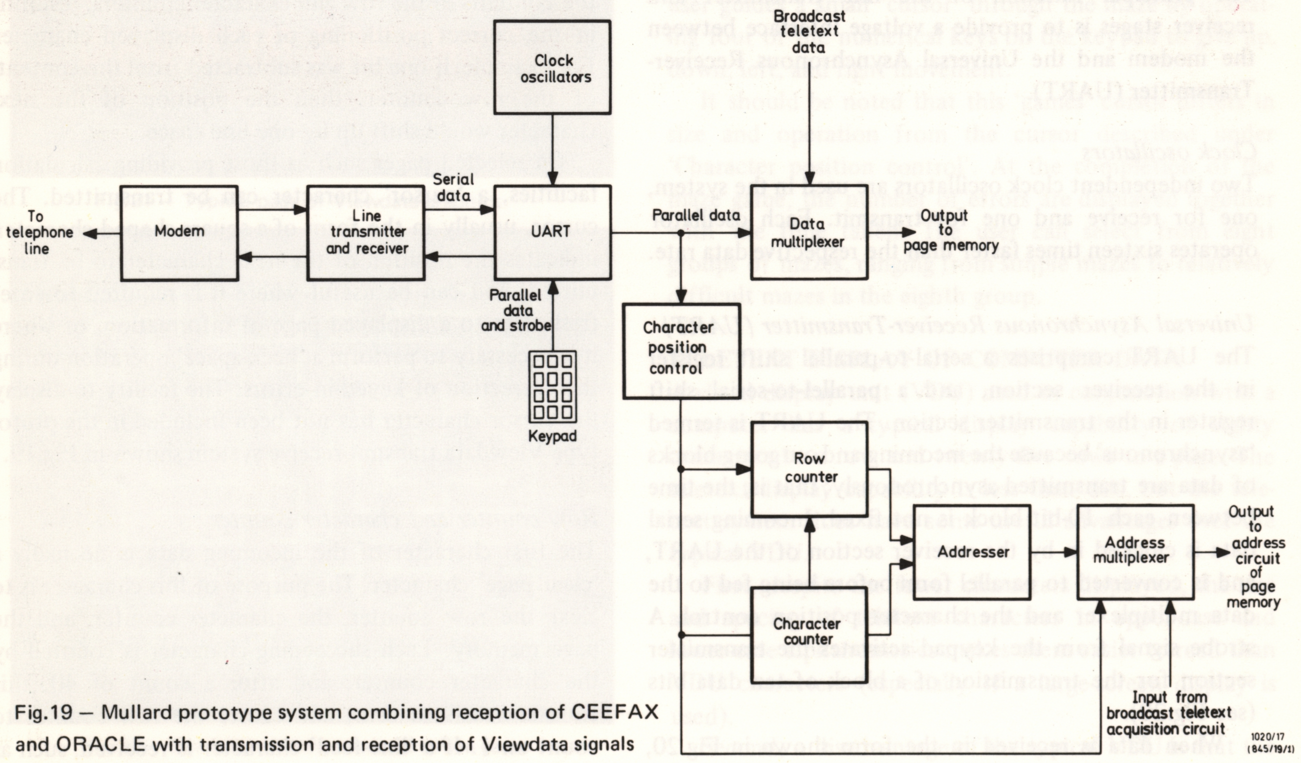


Fig.19 – Mullard prototype system combining reception of CEEFAX and ORACLE with transmission and reception of Viewdata signals

the system accepts addresses from the teletext system and provides an output in the form of addresses for the teletext decoder memory stage. It is therefore possible for the user to switch directly from other forms of teletext to Viewdata operation.

Viewdata modem

The modem used in the prototype system shown in Fig.19 is the Post Office type 1A. This converts the incoming Viewdata audio tones into a digital output for the receiver stage, or the digital output from the transmitter stage into line transmission tones. The serial data output signal from the modem (receiving mode) consists of blocks of ten bits as shown in Fig.20. Each block consists of a start bit, eight information bits including a parity bit, and a stop bit. The pulses comprising the bits swing between the states $+V_M$ (LOW) and $-V_M$ (HIGH), rather than from the LOW state of 0V. The voltage V_M can be fixed at any value between 3 and 20V, relative to 0V.

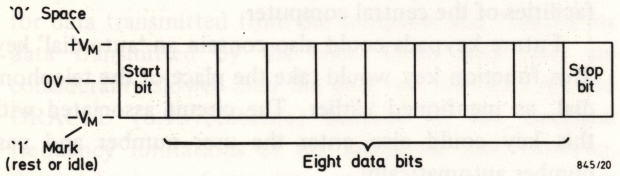


Fig.20 — Viewdata 10-bit output signal block from modem

Line receiver and transmitter stages

The principal function of the line transmitter and receiver stages is to provide a voltage interface between the modem and the Universal Asynchronous Receiver-Transmitter (UART).

Clock oscillators

Two independent clock oscillators are used in the system, one for receive and one for transmit. Each oscillator operates sixteen times faster than the respective data rate.

Universal Asynchronous Receiver-Transmitter (UART)

The UART comprises a serial-to-parallel shift register in the receiver section, and a parallel-to-serial shift register in the transmitter section. The UART is termed 'asynchronous' because the incoming and outgoing blocks of data are transmitted asynchronously; that is, the time between each 10-bit block is not fixed. Incoming serial data is clocked in by the receiver section of the UART, and is converted to parallel form before being fed to the data multiplexer and the character position control. A strobe signal from the keypad activates the transmitter section for the transmission of a block of ten data bits (see Fig.20).

When data is received in the form shown in Fig.20, the UART responds to the leading edge of the start bit and counts eight. After the final count only half of the start bit will have been received, and thus this bit should still be HIGH. The state of the incoming bit is examined at this point, and if the HIGH state is confirmed, then the counter will continue to operate. This verification helps to discriminate between a start bit and transient pulses on the line. The clock pulses are timed to coincide with the middle of each data bit rather than with the leading edges. This method of timing allows for any slight drift that might occur in the clock frequency, and results in positive sampling of the incoming data. (Unlike broadcast teletext, no synchronising information for the clock is contained in the Viewdata transmission.)

It should be noted that the Viewdata system can be operated in full duplex; that is, reception and transmission of data can be carried out at the same time. For example, a Viewdata page can be 'interrupted' during its formation on the television screen if another page number is keyed-in. The partially-formed original page will be replaced by the newly selected page.

Data multiplexer

The data multiplexer switches data from the UART or from the teletext data acquisition stage to the teletext memory.

Character position control

The character position control contains gates which detect incoming control characters. These control characters are used for the addition or subtraction of bits from the contents of the row and character counters, resulting in the correct positioning of each displayed character. For example, if one bit was subtracted from the contents of the row counter, then the position of the next character would shift up by one line space.

On selected pages such as those providing calculation facilities, a 'cursor' character can be transmitted. The cursor, usually in the form of a square-shaped character, indicates the position of the next character to be transmitted, and can be useful where it is required to enter fresh data to a displayed page of information, or where it is necessary to perform a 'back-space' operation during the correction of keyed-in errors. The facility to display the cursor character has not been included in the prototype Viewdata transmit-receive system shown in Fig.19.

Row counter and character counter

The first character of the incoming data is normally a 'clear page' character. The purpose of this character is to clear the row counter, the character counter, and the page memory. Each succeeding character is counted by the character counter, and after a count of 40, this counter resets to zero, and causes the row counter to count on 1. If a 'line-feed' character is received, such as when a row contains less than forty characters, then the row counter automatically counts on 1, so that the succeeding character will appear on the next line.

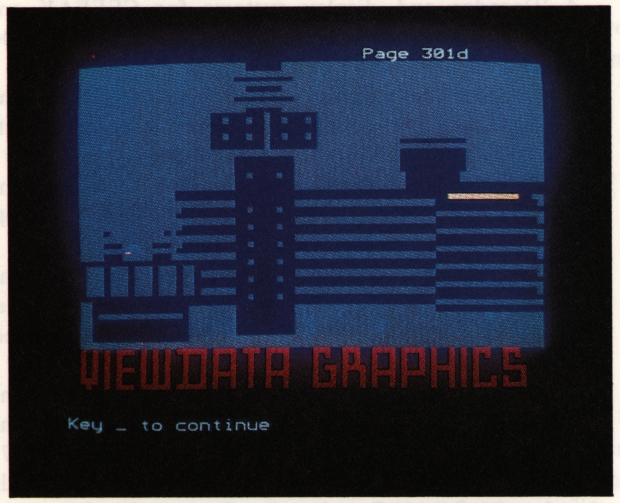
Addresser

The outputs from the two counters are combined to provide a 10-bit binary address for the address multiplexer. This is done by multiplying the contents of the row counter by forty and adding to this total the contents of the character counter. (This process of multiplication is fully described in Ref.3, page 10.) The output from the addresser is fed to the address multiplexer.

Address multiplexer

The address multiplexer selects either broadcast teletext or Viewdata addresses. The prototype system shown in Fig.19 uses the memory and timing chain of the teletext decoder system, and so the address multiplexer is normally switched to the broadcast teletext addresses. After Viewdata operation has been selected by the user, and when a Viewdata character has been received, the address multiplexer is switched to the Viewdata address circuit for a few milliseconds while the Viewdata character is entered. The WOK (Write O.K.) function of the teletext system is activated at the same time.

The output from the address multiplexer is in the form of a 10-bit binary address which is suitable for driving the RAM of the teletext system.


Page 301d

VIEWDATA GRAPHICS

Key _ to continue

Fig.21 — Typical page of Viewdata graphics

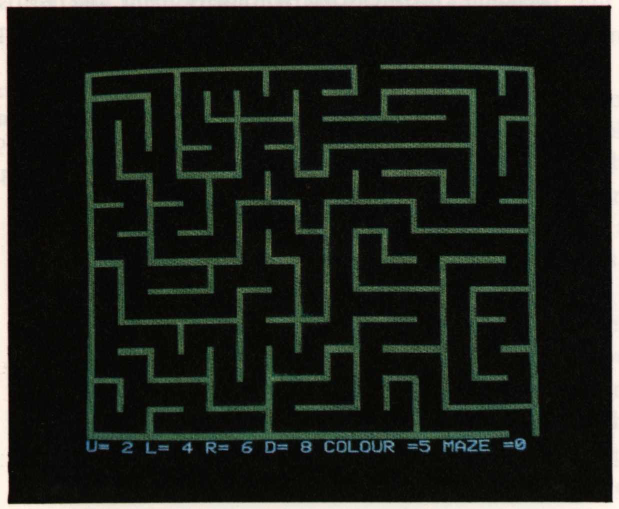

U= 2 L= 4 R= 6 D= 8 COLOUR =5 MAZE =0

Fig.22 — Example of Viewdata interactive game

Viewdata services

Text and graphics can be displayed on the Viewdata pages in the same range of colours provided by broadcast teletext. A typical page of Viewdata graphics is shown in Fig.21. Some of the services envisaged by the Post Office are listed below.

News
Sport
Radio and tv
Going out
Holidays and travel
Tourist guide
Education
Hobbies and pastimes
Jokes, quizzes and games
Home and family help
Marketplace
Cars and motoring
Houses and mortgages
Facts and figures
Money and insurance
Jobs and careers
Business services
Stock markets
Messages
Viewdata index

It can be seen from the above list that whereas some services are fully interactive (such as quizzes or games), other services are purely informative (such as radio and tv). An example of an interactive game is one of the 'mazes' offered by the system, as shown in Fig.22. The user guides a small 'cursor' through the maze by operating four of the numerical keys on the keypad to give up, down, left, and right movement.

It should be noted that this 'games' cursor differs in size and operation from the cursor described under 'Character position control'. At the completion of the maze game, the number of errors are displayed together with the time taken. The user can select from eight groups of mazes, ranging from simple mazes to relatively difficult mazes in the eighth group.

TELETEXT DISPLAY OF COMPUTER DATA

A visual display unit (VDU) used in conjunction with a computer has a typical display capability of eighty characters to a row and twenty-five rows to a page. The teletext display capability is less than this, but the teletext system does have some useful advantages over the typical VDU.

First, despite the fewer characters displayed, the size and spacing of teletext characters in upper-case and lower-case alphanumerics makes them easier to read than VDU characters (especially if a large-screen display is used).

Second, a disadvantage of the typical VDU is that the display is in only one colour. The display of, for example, a block of tabulated data could be made easier to read by breaking up headings, dividing lines, etc., into different colours. The teletext system easily provides this type of display. With the Mullard decoder system, it is possible to display separate halves of a 'page' of data in double-height characters. Because a colour television receiver is used as the display unit, the broadcast reception facility of the receiver can be retained. (Teletext characters can also, if required, be displayed simultaneously with normal tv pictures.) In addition, the teletext system using a television receiver can cost considerably less than a typical VDU.

Some examples of where use could be made of a 'teletext VDU' could include airports, colleges, laboratories, offices, railway stations, and universities.

INTERNATIONAL INTEREST IN TELETEXT

Since the early trials of broadcast teletext in Britain, the interest in this method of data transmission has spread throughout Europe and is now extending to other parts of the world. The British method of transmission is currently being used for exploratory studies and broadcast trials in countries such as Sweden, Germany, and Switzerland. Interest has also been shown by European post office authorities in the Viewdata system and other similar methods of data transmission from a central data bank to the home terminal through the telephone network.

Mullard has played an active part in assisting with the design of teletext systems for use in such countries as Germany, Austria, Denmark, and Sweden. The Mullard prototype teletext decoder itself (Fig.12) has formed the basis of numerous discussions and demonstrations held in several European countries. This decoder, together with a prototype Viewdata decoding system, featured at a symposium held in Sorrento in Italy during September 1976. Those taking part in this symposium included the IBA, RAI (Radiotelevisione Italiana – the Italian television authority), SIP (Societa Italiana Per L'esercizio Telefonico – the Italian telephone authority), and Italian setmakers. Demonstrations were also held at the HEDA (Home Entertainment and Domestic Appliances) exhibition at Birmingham in May 1976, and at the Munich Fair later that year. This type of engagement in international demonstrations and discussions continues to be a part of Mullard activity in teletext, coupled with detailed research in our laboratories.

ACKNOWLEDGEMENTS

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The TDA1071 IC in a.m./f.m. radio receivers

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This article describes the TDA1071 radio IC, and gives details of its application and performance in a.m./f.m. radio receivers.

INTRODUCTION

The TDA1071 is a unique integrated circuit for use in mains and portable radio equipment. The low current consumption and supply voltage, together with a very low peripheral component count, make the IC particularly suitable for portable battery-operated equipment, but it is also suitable for application in mains equipment and car radios.

The integrated circuit incorporates an a.m. oscillator, an a.m. mixer with a.g.c., a four-stage differential amplifier and limiter, and a four-quadrant multiplier. The novelty of the IC lies in the combination of both f.m. and a.m. functions in the multiplier circuit, which acts as a quadrature detector (with squelch) on f.m., and as a synchronous demodulator on a.m.

The use of the TDA1071 in communications receivers has already been described (Ref.1), and this article gives details of a further application in a portable a.m./f.m. receiver. A description of the internal circuit of the TDA1071 is given, and the performance of a prototype receiver described. A brief outline of the application of the IC in mains equipment is also given.

IC CIRCUIT DESCRIPTION

A block diagram of the TDA1071 is shown in Fig.1, and the complete internal circuit in Fig.2; the three main sections are described below.

A.M. oscillator and mixer

The circuit of the a.m. oscillator and mixer (transistors TR_1 to TR_{13}) is substantially the same as that used in the TBA570, details of which are given in Ref.2. The positive supply for this circuit (pin 11) is separate from the main supply to allow decoupling between the oscillator and the main supply on a.m., and to allow the oscillator/mixer circuit to be switched off for f.m. operation.

Amplifier/limiter

The amplifier/limiter section consists of four differential amplifier stages, the outputs from each stage being buffered by emitter-followers; the output of the second stage is brought out to pin 4 via a separate emitter-follower (TR_{38}). The collector resistors of the stages are scaled to give a good limiting characteristic, and stray coupling between stages is minimised by providing a separate buffered supply for each stage (via TR_{47} to TR_{50}). The tail currents for the differential amplifiers and the emitter currents for the emitter-followers are supplied by current sources TR_{14} to TR_{29}, forming a current mirror with TR_{81} and TR_{82}. The d.c. conditions are stabilised by overall d.c. feedback via R_{58}.

Multiplier

Transistors TR_{56} to TR_{59}, TR_{65}, and TR_{66} form a conventional four-quadrant multiplier circuit, supplied

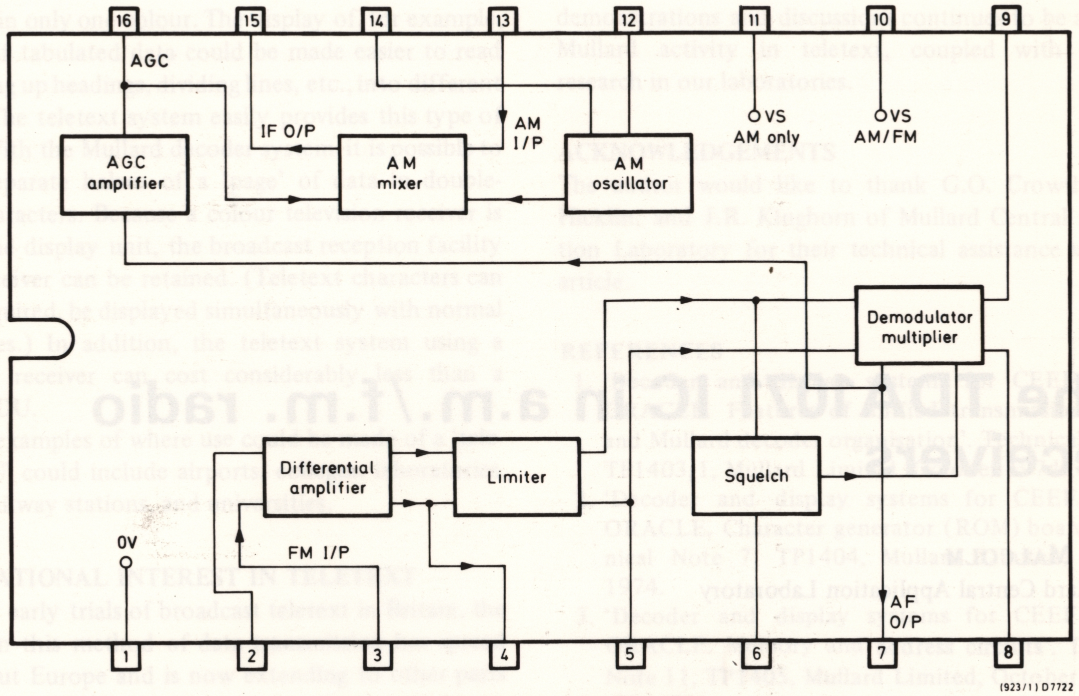


Fig.1 — Block diagram of the TDA1071

by current source TR_{68} acting as a current mirror with TR_{67}. The bases of TR_{56} to TR_{59} are fed by emitter-followers TR_{55} and TR_{60}, the bases of which are brought out to pins 8 and 9. The bases of TR_{65} and TR_{66} are connected to the outputs of the differential amplifier/limiter circuit, and the emitter resistors of these transistors are included to improve circuit balance.

An integrated capacitor (C_1) connects one output of the amplifier/limiter section to pin 9, forming part of the f.m. quadrature detector; pin 9 is also coupled, via an integrated capacitor (C_2), to an a.m. detector/amplifier (TR_{51} to TR_{54}) which drives the squelch transistor (TR_{69}). A small forward bias current for the squelch detector is supplied by TR_{83} to TR_{85}.

The load on the multiplier is provided by two p-n-p current mirrors (TR_{61} to TR_{64}); the output is converted to single-ended form by another current mirror (TR_{72} and TR_{73}), and established at a selected d.c. level ($2 \times V_{be}$) by TR_{74} and R_{50}. This arrangement ensures that the multiplier will operate over a wide range of supply voltages.

POWER CONSUMPTION

The current consumption of the TDA1071 from a 6V supply is detailed below.

Oscillator and mixer	2.8mA	
Amplifier/limiter	3.6mA	(0.9mA for each stage)
Multiplier and stabiliser	5.0mA	
	11.4mA	

PORTABLE RADIO APPLICATION

The TDA1071 is particularly suitable for use in a high-quality portable a.m./f.m. receiver, providing high performance over a wide range of supply voltages and very simple a.m.-to-f.m. switching. The low peripheral component count of the IC is a further advantage, reducing the necessary size of the receiver. The operation, construction, and performance of a laboratory prototype a.m./f.m. receiver using the TDA1071 are described in the following sections. A circuit diagram of the receiver is shown in Fig.3, including both a.m. and f.m. functions.

A.M. operation

The r.f. signal from the ferrite rod aerial (T_5 in Fig.3) is coupled to the base of the mixer (pin 13) via a coupling winding chosen to give an aerial coil working Q-value of about half its unloaded Q-factor. The emitter of the mixer (pin 14) is supplied with an oscillator drive voltage of about 30mV r.m.s. by an oscillator coil injection tap from T_6, and the mixer output at pin 15 is coupled to the input of the differential amplifier (pin 3) via a 470kHz block filter. This filter presents an impedance of about 30kΩ to the mixer, and provides a source impedance of about 100Ω for the integrated differential amplifier.

A.G.C. applied to the mixer restricts the signal level at the second stage of the differential amplifier to the linear region; the carrier level at pin 4 is about 25mV r.m.s. and is determined by the value of the resistor (R_8) between pin 16 and earth. This modulated signal is applied to one input of the multiplier section (pin 8). and the complementary input (pin 9) is decoupled. The

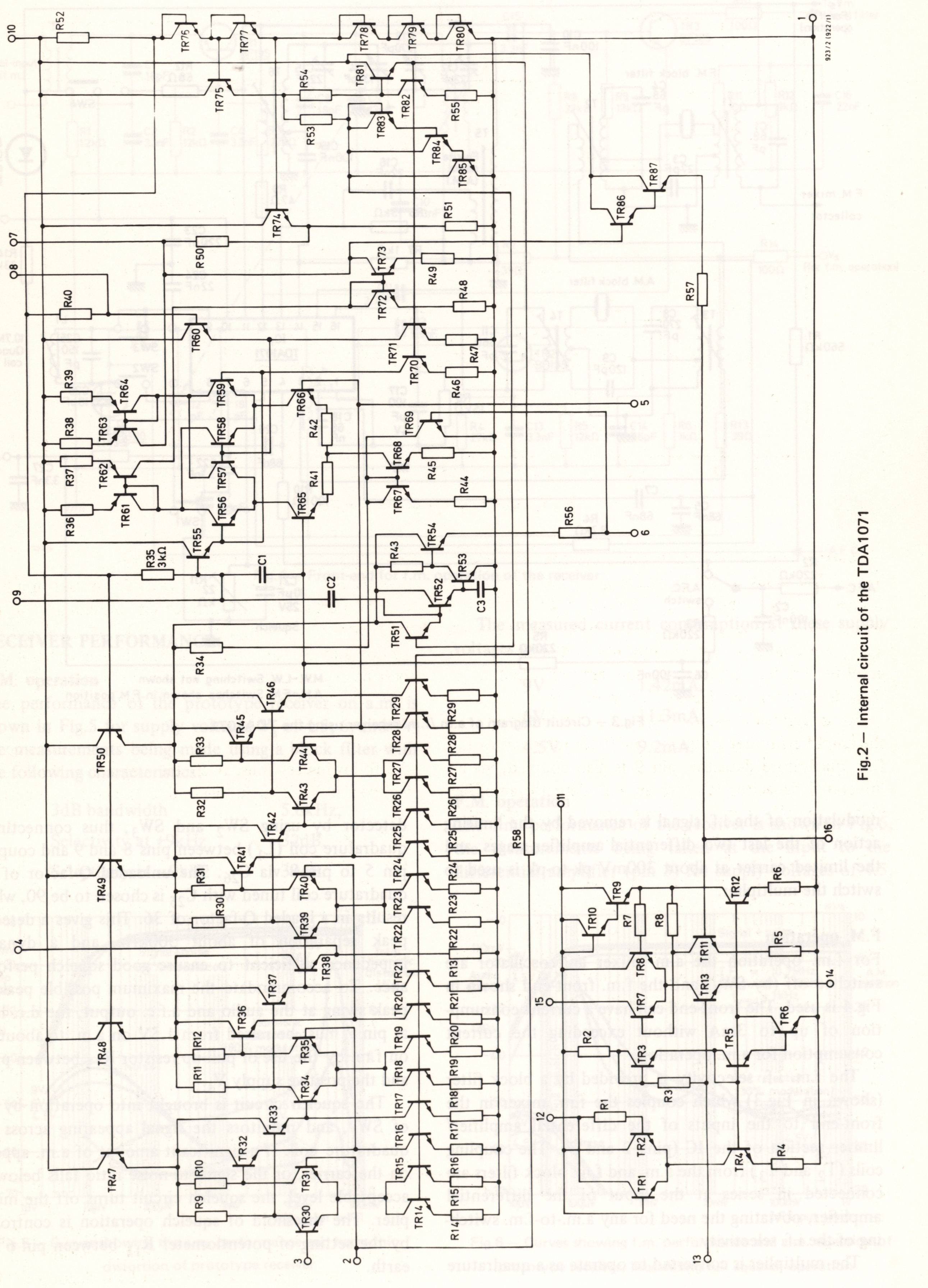
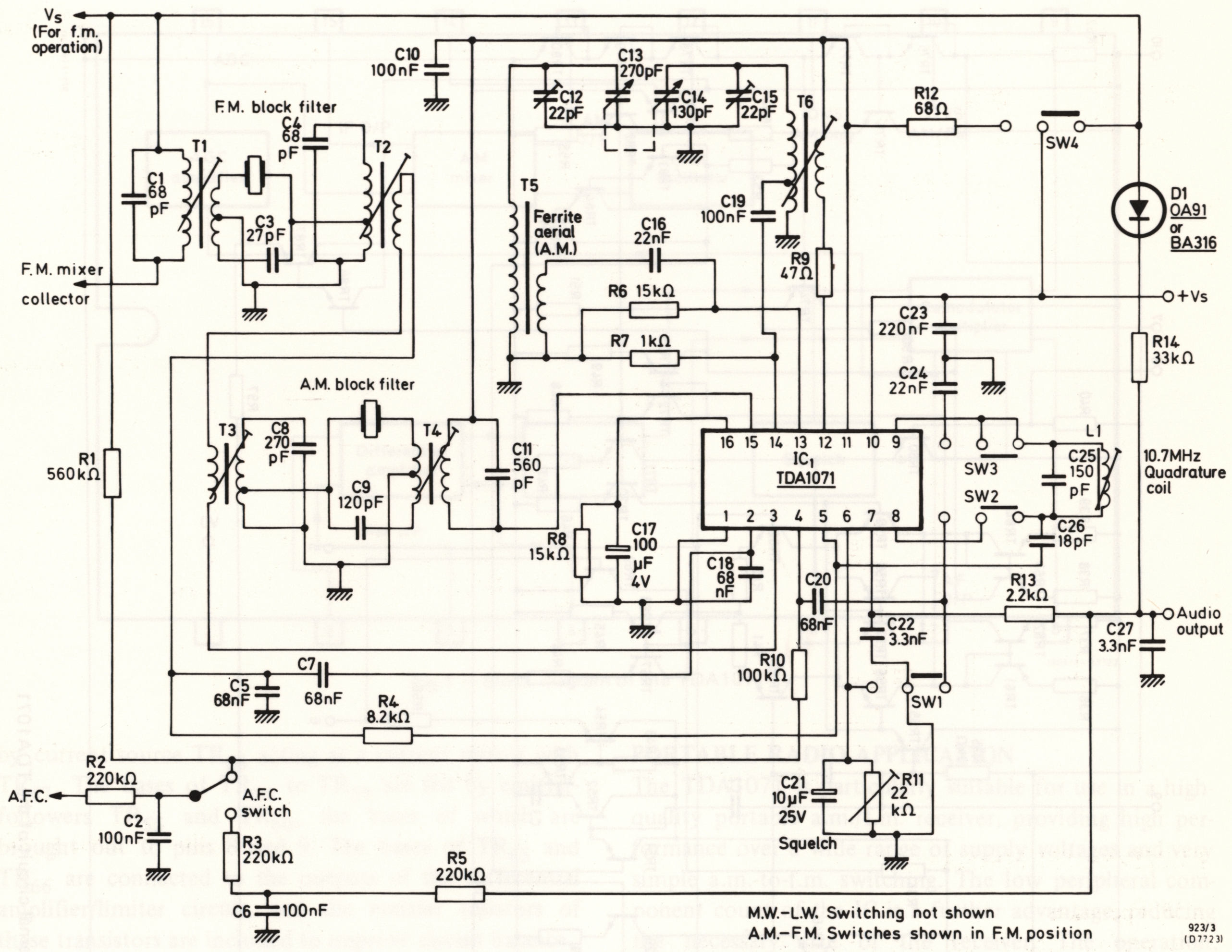


Fig.2 — Internal circuit of the TDA1071



M.W.-L.W. Switching not shown
A.M.-F.M. Switches shown in F.M. position

Fig.3 – Circuit diagram of a.m./f.m. receiver using the TDA1071

modulation of the i.f. signal is removed by the limiting action of the last two differential amplifier stages, and the limited carrier at about 300mV pk-to-pk is used to switch the multiplier.

F.M. operation

For f.m. operation the a.m. mixer and oscillator are switched off (by SW_4) and the f.m. front-end shown in Fig.4 is used. The front-end can have a current consumption of up to 3mA without exceeding the current consumption for a.m. operation.

The f.m. i.f. selectivity is provided by a block filter (shown in Fig.3) which couples the f.m. mixer in the front-end to the inputs of the differential amplifier/limiter section of the IC (pins 2 and 3). The coupling coils (T_2 and T_3) from the a.m. and f.m. block filters are connected in series at the input of the differential amplifier, obviating the need for any a.m.-to-f.m. switching of the i.f. selectivity.

The multiplier is converted to operate as a quadrature detector by using SW_2 and SW_3, thus connecting a quadrature coil (L_1) between pins 8 and 9 and coupling pin 5 to pin 8 via C_{26}. The unloaded Q-factor of the quadrature coil tuned with C_{25} is chosen to be 90, which results in a loaded Q-factor of 36. This gives a detector peak separation of about 300kHz, and a dynamic impedance sufficient to ensure good squelch performance. To accommodate the maximum possible peak-to-peak swing at the audio and a.f.c. output, the d.c. level at pin 7 must be raised from 1.5V on a.m. to about 3V on f.m. by the use of pull-up resistor R_{13} between pin 7 and the positive supply V_s.

The squelch circuit is brought into operation by use of SW_1, and monitors the signal appearing across the quadrature coil. If a significant amount of a.m. appears on the carrier, or the signal-to-noise ratio falls below an acceptable level, the squelch circuit turns off the multiplier. The threshold of squelch operation is controlled by the setting of potentiometer R_{11} between pin 6 and earth.

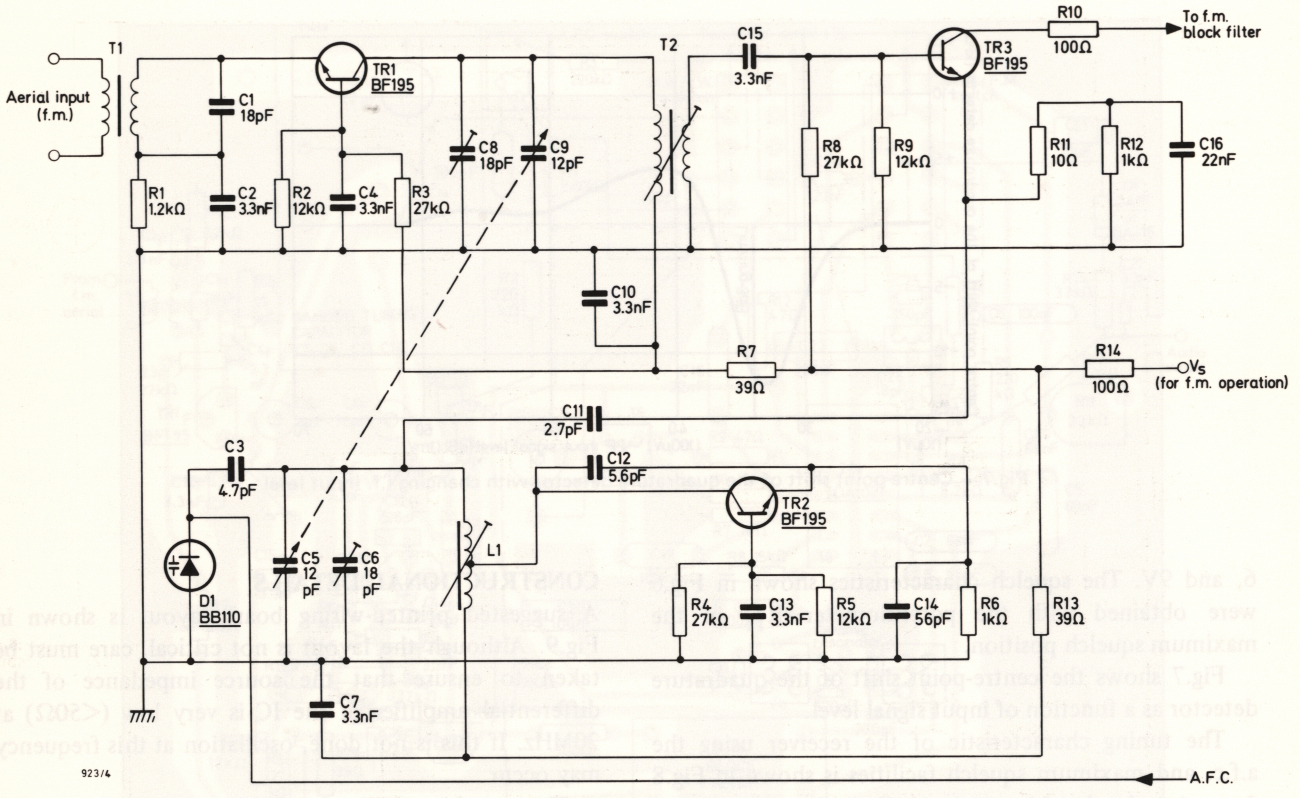


Fig.4 – Front-end for f.m. operation of the receiver

RECEIVER PERFORMANCE

A.M. operation

The performance of the prototype receiver on a.m. is shown in Fig.5 for supply voltages V_s of 4.5, 6, and 9V, the measurements being made using a block filter with the following characteristics:

3dB bandwidth	5.6kHz,
Selectivity at +9kHz	32dB,
Selectivity at −9kHz	30dB.

The measured current consumption at these supply voltages was:

9V	1.42mA,
6V	11.3mA,
4.5V	9.2mA.

F.M. operation

The f.m. performance of the receiver is shown in Fig.6, the measurements being taken at the input to the differential amplifier (pin 3) for supply voltages of 4.5,

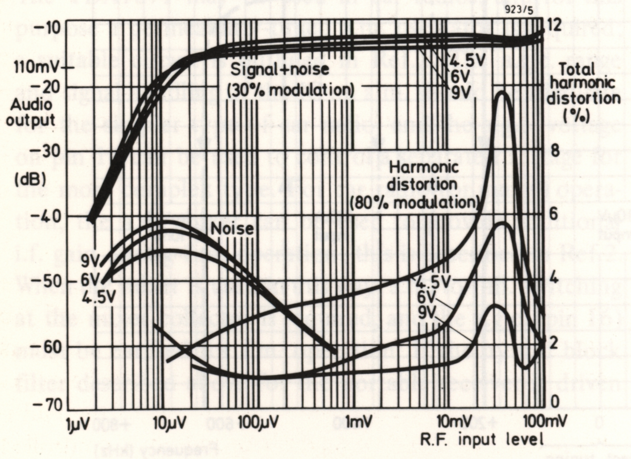


Fig.5 – Curves showing the a.m. performance and harmonic distortion of prototype receiver

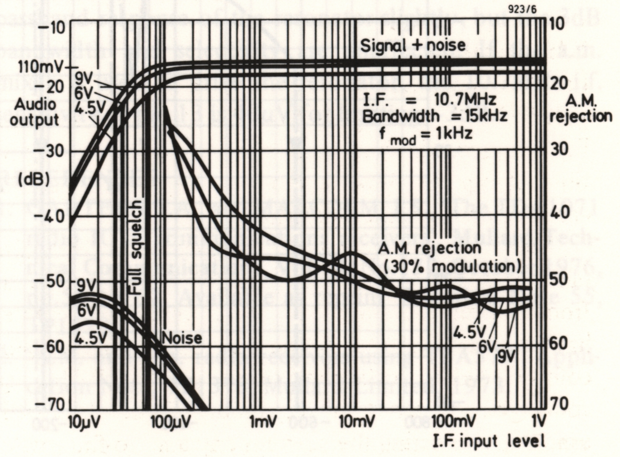


Fig.6 – Curves showing f.m. performance and a.m. rejection of prototype receiver, illustrating full squelch operation

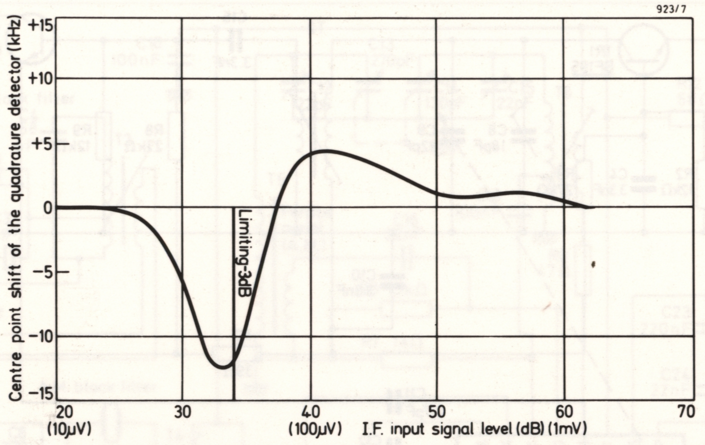


Fig.7 — Centre-point shift of the quadrature detector with changing i.f. input level

6, and 9V. The squelch characteristics shown in Fig.6 were obtained with the potentiometer R_{11} in the maximum squelch position.

Fig.7 shows the centre-point shift of the quadrature detector as a function of input signal level.

The tuning characteristic of the receiver using the a.f.c. and maximum squelch facilities is shown in Fig.8 for various levels of input signal. For this measurement, an f.m. block filter with the following characteristics was used:

3dB bandwidth	170kHz,
Selectivity at +300kHz	35dB,
Selectivity at −300kHz	35dB.

The sensitivity of the complete f.m. receiver is 3µV for limiting −3dB, into an impedance of 75Ω.

CONSTRUCTIONAL DETAILS

A suggested printed-wiring board layout is shown in Fig.9. Although the layout is not critical, care must be taken to ensure that the source impedance of the differential amplifier of the IC is very low (<50Ω) at 20MHz. If this is not done, oscillation at this frequency may occur.

The switching (SW_2 and SW_3) at the inputs of the multiplier (pins 8 and 9) should be arranged as shown in Fig.2, to decouple the quadrature coil as well as pin 9, and so avoid i.f. radiation via C_{25}.

The a.f.c. voltage swing is centred at the d.c. level established on pin 7, so a comparable d.c. level must be provided if a.f.c. switching is required. To ensure that the a.f.c. reference level tracks the d.c. level on pin 7 as the supply voltage varies, the stabilised voltage on pin 4, which is decoupled during f.m. operation, should be used to derive the a.f.c. reference voltage. This connection is included in Fig.3. This stabilised voltage could also be used to provide base bias for the f.m. front-end, which would ensure consistent front-end performance over a range of supply voltages.

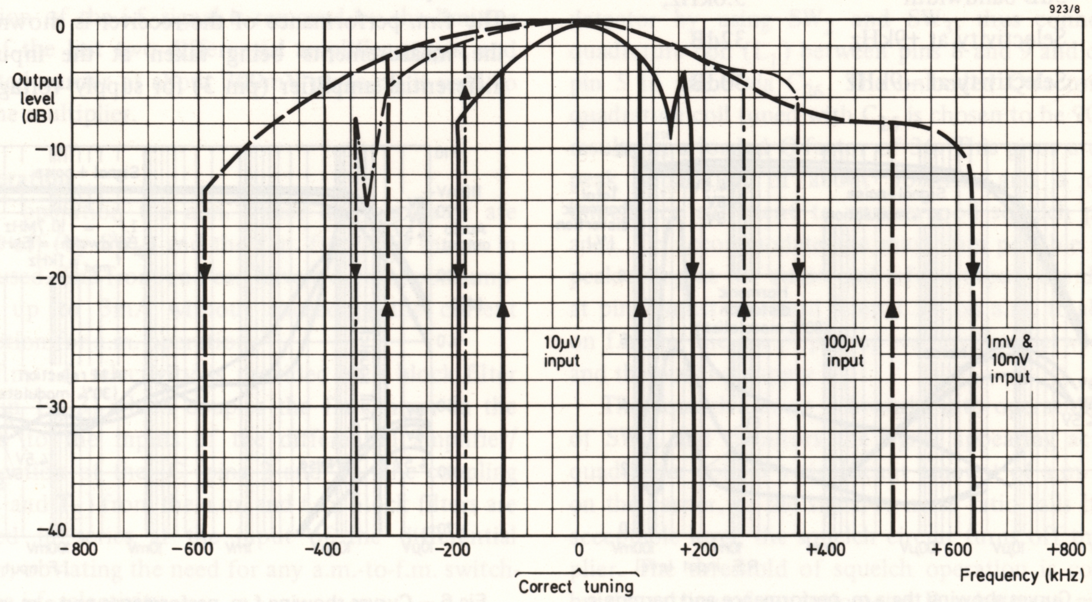


Fig.8 — Tuning characteristic of prototype receiver on f.m., using a.f.c. and full squelch

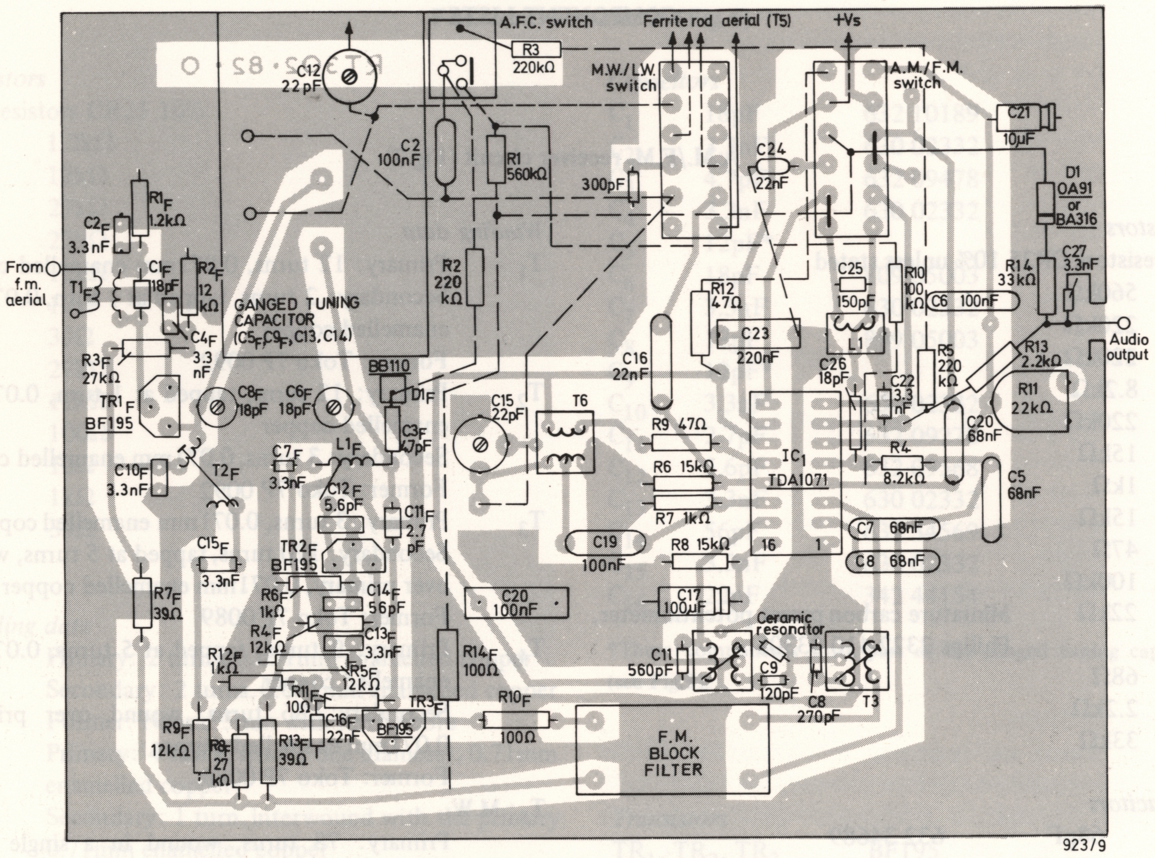

A.F.C. switch
Ferrite rod aerial (T5)
+Vs
R3 220kΩ
C12 22pF
M.W./L.W. switch
A.M./F.M. switch
C21 10µF
C2 100nF
R1 560kΩ
300pF
C24 22nF
D1 OA91 or BA316
C2F 3.3nF
R1F 1.2kΩ
From f.m. aerial
T1F
C1F 18pF
R2F 12kΩ
GANGED TUNING CAPACITOR (C5F, C9F, C13, C14)
R2 220kΩ
R12 47Ω
C25 150pF
R10 100kΩ
C6 100nF
R14 33kΩ
C27 3.3nF
Audio output
C4F 3.3nF
R3F 27kΩ
TR1F BF195
C8F 18pF
C6F 18pF
BB110
D1F
C15 22pF
T6
C16 22nF
C23 220nF
L1
C26 18pF
C22 3.3nF
R5 220kΩ
R13 2.2kΩ
R11 22kΩ
C20 68nF
C3F 47pF
L1F
R9 47Ω
R6 15kΩ
IC1 TDA1071
R4 8.2kΩ
C5 68nF
C10F 3.3nF
T2F
C7F 3.3nF
C12F 5.6pF
C11F 2.7pF
R7 1kΩ
C15F 3.3nF
TR2F BF195
C19 100nF
R8 15kΩ
16
1
C7 68nF
C8 68nF
R7F 39Ω
R6F 1kΩ
C14F 56pF
C20 100nF
C17 100µF
Ceramic resonator
R4F 12kΩ
C13F 3.3nF
R14F 100Ω
C11 560pF
C9 120pF
C8 270pF
T3
R12F 1kΩ
R5F 12kΩ
R11F 100Ω
TR3F
R10F
R9F 12kΩ
R8F 27kΩ
R13F 39Ω
C16F 22nF
BF195
100Ω
F.M. BLOCK FILTER
923/9

Fig.9 — Prototype printed-wiring board layout
Components with the subscript F comprise the f.m. front-end (Fig.4). The 300pF capacitor next to the m.w./l.w. switch is not shown in Fig.3.

ALTERNATIVE APPLICATIONS

The TDA1071 may be used in car radios, and for this purpose a permeability-tuned a.m. oscillator is required; a suitable circuit is outlined in Ref.2. The a.g.c. range and signal handling of the IC on a.m. should be adequate for the simpler type of car radio, and the a.g.c. voltage on pin 16 can be used to control a separate r.f. stage for the more complex type. For car radio (or mains) operation, the a.m. mixer can be used to provide additional i.f. gain during f.m. operation; this is described in Ref.2. When the mixer is used in this way, a.m.-to-f.m. switching at the mixer collector is required, and the a.g.c. (pin 16) must be earthed for f.m. operation. If the hybrid block filter described above for the portable receiver is driven by the a.m. mixer, the 10.7MHz i.f. sensitivity at pin 13 is 5µV for limiting −3dB.

A multi-element ceramic resonator such as the Murata SFE 10.7 can be used to provide i.f. selectivity, but because of the source impedance restraints imposed by the differential amplifier (see earlier) the 330Ω resistive load on the resonator must be bypassed by a 33pF capacitor. The addition of this capacitor modifies the passband response of the resonator slightly, but the 3dB bandwidth and selectivity are unaffected. If the a.m. mixer is used to drive the resonator, the 10.7MHz i.f. sensitivity at pin 13 is 40µV for limiting −3dB.

REFERENCES

1. GARTERS, J.A., and MALCOLM, J.S., 'The TDA1071 radio IC in communications receivers', **Mullard Technical Communications,** Vol.14, No.132, October 1976, pp.54 to 62. Available as reprint Technical Note 55, TP1578.
2. 'A.M. and f.m. radio receivers using TBA570', Application Note, TP1378, Mullard Limited, 1973.

COMPONENT LISTS

A.M./F.M. receiver circuit (Fig.3)

Resistors

All resistors CR25 10% unless stated

R_1	560kΩ	
R_2	220kΩ	
R_3	220kΩ	
R_4	8.2kΩ	
R_5	220kΩ	
R_6	15kΩ	
R_7	1kΩ	
R_8	15kΩ	
R_9	47Ω	
R_{10}	100kΩ	
R_{11}	22kΩ	Miniature carbon preset potentiometer, Philips 2322 410 03308
R_{12}	68Ω	
R_{13}	2.2kΩ	
R_{14}	33kΩ	

Capacitors

C_1	68pF	632 34689
C_2	100nF	342 44104
C_3	27pF	632 34279
C_4	68pF	632 34689
C_5	68nF	342 44683
C_6	100nF	342 44104
C_7	68nF	342 44683
C_8	270pF	632 58271
C_9	120pF	632 34121
C_{10}	100nF	342 44104
C_{11}	560pF	630 02561
C_{12}	22pF	808 11229
C_{13}	270pF*	
C_{14}	130pF*	
C_{15}	22pF	808 11229
C_{16}	22nF	342 44154
C_{17}	100µF, 4V	015 12101
C_{18}	68nF	342 44683
C_{19}	100nF	342 44104
C_{20}	68nF	342 44683
C_{21}	10µF, 25V	015 16109
C_{22}	3.3nF	630 02332
C_{23}	220nF	342 44224
C_{24}	22nF	342 44154
C_{25}	150pF	632 34151
C_{26}	18pF	632 10189
C_{27}	3.3nF	630 02332

*These components form part of the ganged tuning capacitor (see Fig.9).

Winding data

T_1	Primary: 12 turns, 0.071mm enamelled copper Secondary: 2 turns, tapped at 1 turn, 0.071mm enamelled copper Former: Toko 7P 0092
T_2	Primary: 12 turns, tapped at 1 turn, 0.071mm enamelled copper Secondary: 3 turns, 0.071mm enamelled copper Former: Toko 7P 0092
T_3	Primary: 3 turns, 0.071mm enamelled copper Secondary: 120 turns, tapped at 5 turns, wound over primary, 0.071mm enamelled copper Former: Toko 7P 0089
T_4	Primary: 9 turns, tapped at 5 turns, 0.071mm enamelled copper Secondary: 86 turns, wound over primary, 0.071mm enamelled copper Former: Toko 7P 0089
T_5: M.W.	Primary: 78 turns, wound in a single layer, 3 × 3 × 3 × 0.063mm litz Secondary: 4 turns, wound over the earthy end of the primary, 3 × 3 × 3 × 0.063mm litz
: L.W.	Primary: 210 turns, wave-wound, 9 × 0.063mm litz Secondary: 12 turns, wound under the primary, 9 × 0.063mm litz

For T_5 the coils are mounted on a ferrite rod, 178mm in length, diameter 9.5mm.

L_1	8 turns, 0.071mm enamelled copper, Former: Toko 7P 0092

Switch

SW_1 to SW_4 Lipa and Isostat 4-pole 2-way switch

Integrated circuit

IC_1 TDA1071

F.M. front-end circuit (Fig.4)

Resistors

All resistors CR25 10%

R_1	1.2kΩ
R_2	12kΩ
R_3	27kΩ
R_4	27kΩ
R_5	12kΩ
R_6	1kΩ
R_7	39Ω
R_8	27kΩ
R_9	12kΩ
R_{10}	100Ω
R_{11}	10Ω
R_{12}	1kΩ
R_{13}	39Ω

Winding data

T_1	Primary: 2 turns, 0.031mm enamelled copper Secondary: 2 turns, 0.031mm enamelled copper Former: Neosid 5mm with ferrite core
T_2	Primary: 4 turns, spaced one diameter, 0.71mm enamelled copper Secondary: 1 turn, interwound with the primary 0.71mm enamelled copper Former: Neosid 5mm with ferrite core
L_1	3 turns, spaced one diameter and tapped at 1½ turns, 0.71mm enamelled copper Former: Neosid 5mm with ferrite core

Capacitors

C_1	18pF	632 10189
C_2	3.3nF	630 02332
C_3	4.7pF	632 09478
C_4	3.3nF	630 02332
C_5	12pF*	
C_6	18pF	809 05003
C_7	3.3nF	630 02332
C_8	18pF	809 05003
C_9	12pF*	
C_{10}	3.3nF	630 02332
C_{11}	2.7pF	632 09278
C_{12}	5.6pF	632 09568
C_{13}	3.3nF	630 02332
C_{14}	56pF	632 34569
C_{15}	3.3nF	630 02332
C_{16}	22nF	342 44154

*These components form part of the ganged tuning capacitor (see Fig.9).

Transistors

TR_1, TR_2, TR_3	BF195

Diode

D_1	BB110

Product Information: System design aids for the 2650 microprocessor

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Mullard Central Technical Services

INTRODUCTION

Microprocessors are beginning to be used in rapidly increasing numbers to replace conventional 'hard-wired' logic control systems, a development which has become feasible with the production of economic LSI chips incorporating the control and processing sections of a general-purpose microcomputer. This technological advance has made the replacement of specialised logic systems by more versatile program-controlled systems economical as well as desirable.

The main advantages of using microprocessors for control are enhanced flexibility and reduced modification and design times. These arise because of the inherent nature of a microprocessor system. The specialisation of such a system lies in the program used, which controls general-purpose processor and memory circuits, rather than in the physical interconnection of logic functions. For this reason the microprocessor and its associated memory and interface units may be used in various applications, the only change necessary being the substitution of one control program by another. This can be done by replacing the PROMs storing the program with newly programmed PROMs, or by reprogramming EPROMs if these units are in use. Modification of a system is also simplified, as only the program in PROM must be modified, rather than large numbers of logic gates and connections.

However, before a microprocessor control system can be implemented, the program to be used must be fully tested and corrected before being commited to PROMs for final installation. When selecting a microprocessor, therefore, the designer must consider not only the performance of the microprocessor and its associated peripheral circuits, but also the range of program design and development aids provided. The Signetics IC marketing group of Mullard has introduced a wide range of such aids to assist users of the 2650 microprocessor, and this article gives a brief description of the 2650 and its hardware support. General descriptions and specifications of these design aids are given in Ref.1, and more detailed information is available in Refs.2 to 19.

THE 2650 MICROPROCESSOR

The Signetics 2650 (Fig.1) is a single-chip 8-bit parallel processor, incorporating 576 bits of ROM, about 250 bits for registers, and about 900 integrated logic gates. These functions are implemented by use of the ion-implanted n-channel silicon gate MOS technology; this method of construction provides a combination of high function density, low threshold voltage, moderate speed, and good manufacturing yields. The main features of the 2650 are described in the following sections; further details are given in Ref.2.

Physical characteristics

The processor chip is encapsulated in a standard 40-pin dual-in-line package, and requires only one +5V supply and one clock input. The maximum current consumption is 105mA at 5V, this low value being made possible by the technology used in the construction of the chip. The clock input accepts standard TTL levels, and can be of any frequency up to a maximum of 1.25MHz. This feature permits single-stepping of the clock, facilitating the checking of a system, and also provides a simple method of halting the processor.

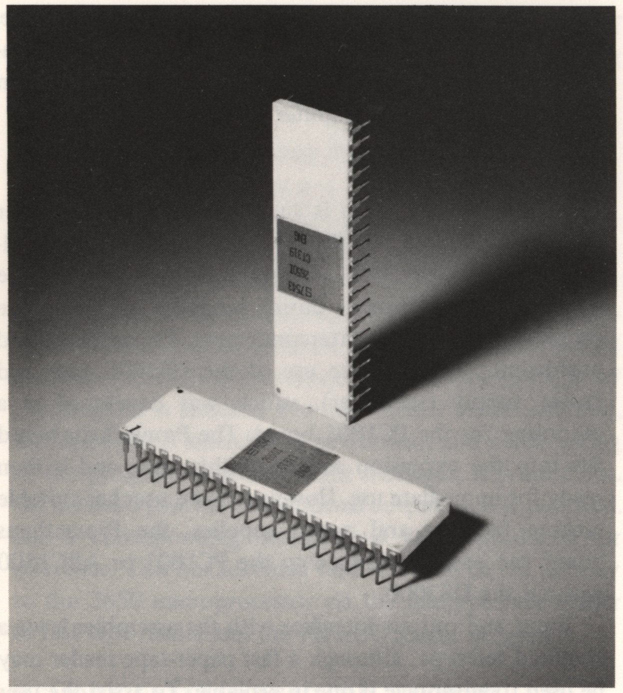
Fig.1 — 2650 microprocessors

Processor architecture

The 2650 has an internal parallel 8-bit structure, and includes an 8-bit bidirectional tri-state data bus and a separate 15-bit tri-state address bus giving an addressing range of 32 768 bytes of memory. Seven general-purpose 8-bit registers are provided on the chip; a 16-bit register called the Program Status Word (PSW) is also provided, and this holds status and control bits which may be loaded, stored, preset, or cleared using various processor instructions. The PSW gives the 2650 exceptional flexibility and processing power by making status information readily available to the programmer, and by allowing the user to control the processor by setting bits in the PSW.

When the processor is required to service external devices, it is desirable to have a mechanism whereby the processor can be interrupted and the service routine initiated whenever the external device is ready. The 2650 has a single-level hardware vectored interrupt capability; when an interrupt occurs the processor finishes the execution of the current instruction and then branches to the service routine, which can be anywhere in memory, to service the interrupting device.

2650 interfacing

The 2650 inputs and outputs are designed to be compatible with standard widely available logic families such as TTL, CMOS, and low-power STTL; this includes the single-phase clock input described earlier, which saves the cost of high-level multiphase clock-driver circuitry. As many MSI circuits and LSI interface and memory circuits (for example, the Signetics 825 and 8T series) have low-current p-n-p buffered STTL inputs, these circuits are recommended for use in 2650 systems.

One of the most important interface characteristics of the 2650 is its ability to operate in a system using industry-standard memories, for example 1024 × 1 and 256 × 4 n-channel RAMs and 1024 × 8 n-channel ROMs. These memories are widely available in large numbers, giving reduced system cost compared with non-standard memories. The 2650 operates successfully with memories of any access time, because of the completely asynchronous interface provided in the processor for this purpose. However, memories with an access time of 1μs or less allow the processor to operate at maximum speed.

Similarly, standard input and output circuits may be used. As for the memory interfaces, the input and output can operate in a completely asynchronous manner, and for this reason devices operating at any speed up to the maximum data transfer rate may be connected without buffering. Data paths are driven with tri-state buffers, allowing multiprocessor and direct memory access configurations to be designed; there is a serial input/output path transferring data sequentially, and 8-bit data paths transferring data in parallel.

2650 instruction set

The instruction set of a microprocessor is the range of coded instructions, available to the user, which the processor can execute. The 2650 has 75 such instructions: about 40% of these are arithmetic and logical instructions (Boolean, arithmetic manipulation, and compare), each of which may be executed in eight possible addressing modes; about 30% are branch instructions incorporating six addressing modes; and the remaining 30% includes input/output instructions, PSW operations, and the HALT instruction, among others. Each instruction is up to 3 bytes long, depending on the instruction and addressing mode used.

This large variety of instructions and addressing modes makes the 2650 very versatile, and the instructions are typical of those available for larger computers.

2650 PROTOTYPE BOARDS – PC1001 AND ABC1500

As mentioned earlier, a microprocessor includes the control and processor units of a computer, and needs to be interfaced to memory and input/output devices before a program can be run on it. The PC1001 and ABC1500 (Refs.3 and 4) are printed-wiring boards containing microcomputer systems based on the 2650 and compatible Signetics memory and input/output circuits, and have been designed to assist the user to develop and debug prototype programs. Both boards are fundamentally the same, differing only in memory capacity and in the arrangement of input and output, and they perform the same function. They both include the PIPBUG control and debug program (Ref.5) stored in 1k of PROM, and RAM memory (1k for the PC1001, ½k for the ABC1500) to store the user's program; they both have parallel and serial input/output ports (1 serial, 2 parallel input and 2 parallel output for the PC1001; 1 serial, 2 parallel input/output for the ABC1500) to interface with peripheral devices.

In operation, the user's program is punched in hexadecimal form (where 1 digit represents 4 bits) on paper tape, and loaded into RAM by use of the PIPBUG loader program and a teletype or fast reader. The program can then be run on the 2650, controlled via PIPBUG, and the output and status information is available on the edge connector of the board for connection to indicators to illustrate the progress of the program. PIPBUG enables the programmer to select breakpoints in the program, at which the run stops and status information can be checked; it also allows the modification of the program in RAM and the dumping of the corrected program onto a new paper tape for use in blowing PROMs.

The PC1001 and ABC1500 are versatile aids allowing the testing and correction of small-scale programs, using PIPBUG, and saving considerable time in program development.

2650 RESIDENT ASSEMBLER PC1600SC – PROMETHEUS

Any processor unit, large or small, can understand only instructions and data supplied to it in binary form. If, say, the user writes a series of instructions in English and the data to be processed in normal decimal form, both sets of information must be converted to binary form before the processor can perform the specified operations on the data.

To perform this conversion, various computer programs called assemblers have been developed. These enable the user to write programs in which each instruction is represented by a mnemonic which suggests the definition of the instruction; for instance the mnemonic ADDZ may represent an 'add' instruction. The inclusion of data is also simplified, as the user can specify which form is to be used, such as decimal or octal. An entire series of mnemonics representing instructions is called an assembly language, and an assembler program is designed to take assembly language instructions as input and produce as output the same sequence of instructions in a form suitable for direct input to the processor.

There are three main alternatives open to the user of a microprocessor who wishes to make use of an assembler:

- to use a ready-written assembler program, on cards or tape, if a large computer is available;
- to use computer time in the time-sharing system of a large installation;
- to use a resident assembler program stored in system hardware.

Prometheus (Ref.6) is an example of the third alternative, and because of its simplicity of construction and operation, Prometheus makes program assembly possible in the simplest of microcomputer systems.

System hardware

The Prometheus system is supplied with the assembler program stored in 11 PROMs mounted on a printed-wiring board; 16 RAM ICs are also mounted on the board for use as storage during program assembly. The simplest method of interconnecting Prometheus and prototyping board is the use of the DS2000 base and power supply (see later), which was developed as a mounting for the PC1001 board. The Prometheus board fits into the extension socket of this base, and is then ready for immediate use. However, if the user has suitable racking facilities and power supplies, the Prometheus board can easily be linked to the PC1001 or ABC1500 without the DS2000.

Input and output interface with the assembler is via a standard teletype, although a fast paper-tape reader may be used to advantage if one is available. To assist the user who wishes to employ a fast reader, an extra socket has been included on the Prometheus board for a PROM containing a tape-reader control program.

The Prometheus assembler program

Prometheus is designed for use with the PC1001 or ABC1500 prototyping boards, both of which include the PIPBUG control program; this includes a loader program which accepts input in hexadecimal form (in which each digit represents four binary digits) and converts it to binary form for input to the 2650 processor unit. For this reason the Prometheus assembler program does not need to convert the assembly language input to binary but only to hexadecimal form which is then fed into the 2650 via PIPBUG.

Prometheus accepts 2650 assembly language instructions as input, and provides the same facilities as are available in other 2650 assembler programs such as PIPASM, except the capacity for handling EBCDIC constants, which are normally used only in large installations. In addition, the Prometheus program offers some new features to the user. An important feature of the Prometheus assembler is the predefinition of 20 common symbols, in addition to the 365 symbols which the user can define in a program to be assembled. Four new error messages are also provided, to supplement those already available on other 2650 assemblers and give further assistance to the programmer in identifying mistakes in logic or assembly language 'grammar'.

Another important addition is a new assembler directive, which has been added to make it possible for a single program to be made up of several separate assembly language tapes, which are then assembled on to a single hexadecimal tape. In this way corrections to a part of the program necessitate the replacement of only a short section of tape rather than the whole program tape.

Assembling a program using Prometheus

The Prometheus program is a three-pass assembler; that is, the entire assembly language tape is passed through the teletype and scanned by the assembler three times. On the first pass, all the symbols defined by the user are stored in the RAMs on the Prometheus board, and simple errors such as invalid symbols or repetition of a symbol are detected. During the second pass, the internal logic of the program is checked and any further errors detected, the line-by-line assembly is performed, and a full listing of the program, including error messages, is printed out. On the third pass the hexadecimal output tape is punched. and a corresponding hexadecimal listing produced for reference. This hexadecimal tape can then be fed directly to the 2650 microprocessor via the teletype tape reader or fast tape reader and the PIPBUG loader program.

MEMORY EXTENSION BOARD – PC2000

The PC2000 is a 4k memory board designed to be compatible with the 2650, and comprises 32 NMOS 1024 × 1 static RAMs organised in four groups of 1024 bytes each. Decoding is provided to select one of the four groups, and also to distinguish a particular board when more than one is used. In a system of up to eight boards, each one is uniquely identified by wire jumpers, and no external decoding is required.

The PC2000 is fully compatible with the PC1001 and ABC1500, and may typically be used to extend the RAM memory of these boards when testing large prototype programs. The memory board requires a single +5V supply, and is TTL-compatible, with tri-state drivers and receivers for the data bus.

MOUNTING-BASE AND POWER SUPPLY – DS2000

All the printed-wiring boards described above can be mounted on a racking system designed and made by the user, but this can be a time-consuming and inconvenient process. One method of mounting and powering the boards is to use the DS2000 base (Ref.7), which has two 100-pin sockets and six other sockets; the first two for mounting the PC1001, ABC1500, PC2000, or Prometheus, as required, and the remainder for making signals from these boards more easily available to the user. These signals include all the input/output signals, making interconnection with a teletype, for example, much easier.

The DS2000 also includes four sets of LED indicators, displaying the information on the address bus, the data bus, and the two non-extended input/output ports. These can be used in conjunction with the RUN/PAUSE and STEP control switches on the base to monitor the execution of a program. With the RUN/PAUSE switch on PAUSE, the STEP switch causes the processor to execute one instruction when it is pressed, and then wait. The LED indicators can then be used to check the information on the address bus, data bus, and the output ports after the execution of the instruction. In this way the operation of the program can be checked.

2650 TESTWARE INSTRUMENT – TWIN

The program development aids described so far have been designed for small-scale programs and systems. For larger and more complex systems the TWIN system (Ref.8) offers many advantages to the programmer.

A typical TWIN system consists of three hardware elements; a Prototype Development Controller (PDC), a floppy-disc storage subsystem, and a system console (typically a CRT terminal). The PDC includes a bipolar and MOS PROM programmer, besides an in-circuit emulation/hardware debug facility. A wide range of PDC boards and system peripherals are available.

Software includes an Operating System, File Management, Debug Software, a Text Editor, and a 2650 Resident Macro Assembler. These programs are stored on the floppy disc unit, and simplify software development.

The TWIN system introduces a powerful multiprocessor architecture, using one 2650 as an operating system controller which is completely independent from the slave 2650 which is used to test the user's program. There is 16k of common memory for the two microprocessors, which may be extended to 64k. Hardware interfaces and software drivers are provided for the floppy disc unit, a teletype, a CRT terminal, a fast paper-tape reader, a line printer, and an RS232 (V24) terminal.

The TWIN thus enables the user to write, assemble, test, debug, and edit programs, and transfer them to PROMs for final installation, using only one hardware system, giving a versatile and efficient service to the designer.

TECHNICAL SUPPORT AND DOCUMENTATION

Support for the user of the 2650 is provided by a large number of applications engineers throughout Europe, providing a technical back-up service via the Signetics marketing group. This service is another important aid in system development and problem-solving, and includes an expanding range of technical documents which are listed in Refs.9 to 19.

REFERENCES

1. 'Signetics 2650 Introductory Brochure and Short Form Catalogue' (order code 9399 509 55361).
2. 'Introducing the 2650' (order code 9399 509 51261).
3. '2650 Evaluation Printed Circuit Board Level System (PC1001)', Signetics Microprocessor Document SP50.

4. 'The ABC1500 Adaptable Board Computer', Signetics Microprocessor Document SP55.
5. 'PIPBUG', Signetics Microprocessor Document SS50.
6. 'Prometheus: Resident Assembler PC1600SC for the 2650 Microprocessor', Technical Note 60, TP1592/1, Mullard Limited, 1977.
7. '2650 Demo Systems', Signetics Microprocessor Document SP51.
8. Signetics TWIN Manual.
9. 'Serial Input/Output', Signetics Microprocessor Document AS50.
10. 'Bit and Byte Testing Procedures', Signetics Microprocessor Document AS51.
11. 'General Delay Routines', Signetics Microprocessor Document AS52.
12. 'Binary Arithmetic Routines', Signetics Microprocessor Document AS53.
13. 'Conversion Routines', Signetics Microprocessor Document AS54.
14. 'Support Software for use with the NCSS Timesharing System', Signetics Microprocessor Document SP52.
15. 'Simulator, Version 1.2', Signetics Microprocessor Document SP53.
16. 'Support Software for use with the General Electric Mark III Timesharing System', Signetics Microprocessor Document SP54.
17. 'Absolute Object Format (Revision 1)', Signetics Microprocessor Document SS51.
18. '2650 Initialisation', Signetics Microprocessor Document MP51.
19. 'Low Cost Clock Generator Circuits', Signetics Microprocessor Document MP52.

All these Signetics publications are available from Mullard Limited.

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Simple temperature sensing circuits using thermistors (pp.77 to 82)

Since the publication of this article, the 'two-point' thermistors types 2322 640 90002 and 2322 640 90003 have been withdrawn. They have been replaced by new types, 2322 640 90015 and 2322 640 90013 respectively, with somewhat different characteristics. The properties of the old and new types are compared in the following tables.

All other properties of the old and new types are identical. Please note, however, that the difference in the resistance/temperature characteristics prevents the new types being used as direct replacements for the 2322 640 90002 and 2322 640 90003 in the circuits described in the article. The circuits may, however, be modified to accept the new types.

The other two types mentioned in the article, the 2322 640 90004 and 2322 640 90005, continue to be available.

Old type 2322 640 90002		New type 2322 640 90015	
Resistance at −20°C	8.6kΩ ±8%	Resistance at −20°C	27kΩ approx.
Resistance at −10°C	5.3kΩ approx.	Resistance at −10°C ±1.5°C	15kΩ
Resistance at 0°C	3.5kΩ approx.	Resistance at 0°C	8kΩ approx.
Resistance at 25°C	1.215kΩ ±7%	Resistance at 25°C ±1.5°C	2.7kΩ

Old type 2322 640 90003		New type 2322 640 90013	
Resistance at −30°C	13.35kΩ ±5%	Resistance at −30°C ±1.5°C	50kΩ
Resistance at −20°C	8.0kΩ ±4%	Resistance at −20°C ±1.5°C	27kΩ
Resistance at −10°C	5.0kΩ ±4.5%	Resistance at −10°C ±1.5°C	15kΩ